2*30W I²S Input Stereo Class D Amplifier

FEATURES

- Power supply: 4.5V - 26V
- Audio Performance
  - Output Power (BTL)
    2×30W (PVDD=24V, R_L=8Ω, THD+N=1%)
  - Output Power (PBTL)
    60W (PVDD=24V, R_L=4Ω, THD+N=1%)
  - THD+N=0.02% (PVDD=24V, R_L=8Ω, Po=1W)
  - Noise: 75uV (Gain = 25.2dB, A weighted)
  - Efficiency: 91 % (PVDD=12V, R_L=4Ω, Po=10W)
- Audio I/O Configuration
  - Single Stereo I²S Input
  - BTL or PBTL output
  - 32, 44.1, 48, 88.2, 96kHz Sample Rates
- General Operational Features
  - Selectable Hardware or I²C Control mode
  - Integrated Digital Output Clipper and AGC
  - Integrated Thermal Foldback Function
  - Programmable I²C Address (110110x[R/W])
  - Adjustable Switching Frequency for Class D
- Robustness Features
  - Clock Error, DC, and Short-Circuit Protection
  - Overtemperature and Programmable Overcurrent Protection
- Packages
  - Pb-free Packages, QFN36L

APPLICATIONS

- Bluetooth/Wi-Fi Speakers
- Portable Speakers
- Smart speakers
- LCD TV/Monitor
- Sound Bars, Docking stations, PC Audio

DESCRIPTION

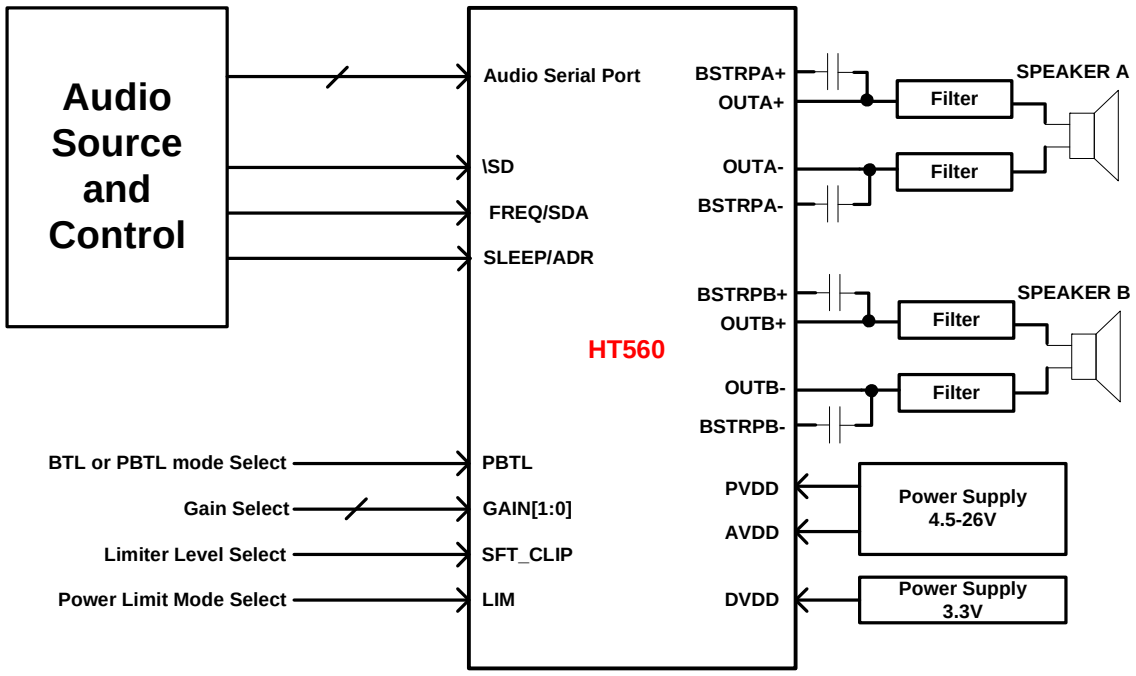
The HT560 is a stereo Class D audio amplifier with an I²S input serial port. It supports a variety of audio clock configurations via two speed modes.

The outputs of the HT560 can be configured to drive two speakers in stereo BTL mode or mono PBTL mode.

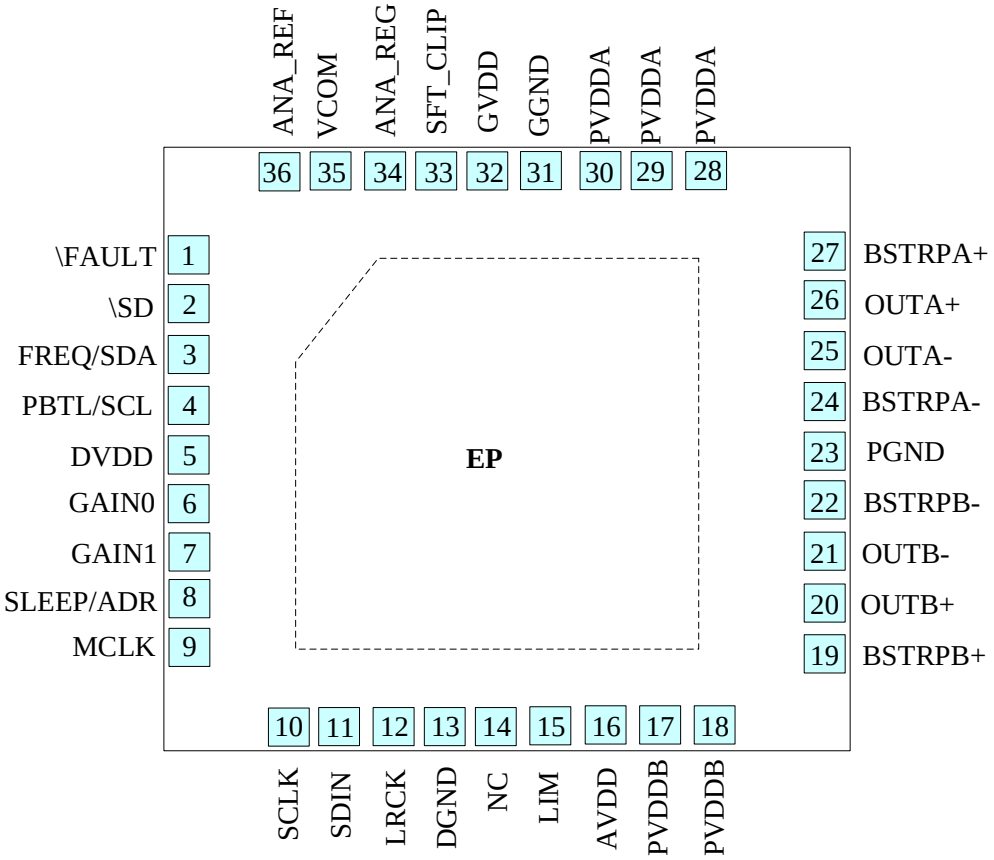
The HT560 also includes hardware and I²C control modes, integrated digital clipper, AGC, several gain options, and a wide power supply operating range to enable use in a multitude of applications.

An optimal mix of thermal performance and device cost is provided in the 110-mΩ $R_{DS(ON)}$ of the output MOSFETs. Additionally, a thermally enhanced 36-Pin QFN provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

TYPICAL APPLICATION



■ TERMINAL CONFIGURATION



Top View

■ TERMINAL FUNCTION

Terminal No.	Name	I/O*1	Description
1	\FAULT	O	Speaker amplifier fault terminal, which is pulled LOW when an internal fault occurs
2	\SD	I	Places the speaker amplifier in shutdown mode while pulled down.
3	FREQ/SDA	I	Dual function pin that functions as an I²C data input pin in I²C Control Mode or as a Frequency Select terminal when in Hardware Control Mode.
4	PBTL/SCL	I	Dual function pin that functions as an I²C clock input terminal in I²C Control Mode or configures the device to operate in pre-filter Parallel Bridge Tied Load (PBTL) mode when in Hardware Control Mode.
5	DVDD	P	Power supply for the internal digital circuitry
6	GAIN0	I	Adjusts the LSB of the multi-bit gain of the speaker amplifier
7	GAIN1	I	Adjusts the MSB of the multi-bit gain of the speaker amplifier
8	SLLEP/ADR	I	In Hardware Control Mode, places the speaker amplifier in sleep mode. In I²C Control Mode, is used to determine the I²C Address of the device
9	MCLK	I	Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking
10	SCLK	I	Bit clock for the digital signal that is active on the serial data port's input data line
11	SDIN	I	Data line to the serial data port

12	LRCK	I	Word select clock for the digital signal that is active on the serial port's input data line
13	DGND	G	Ground for digital circuitry (NOTE: This pin should be connected to the system ground)
14	NC	-	Not connected inside the device (all "no connect" pins should be connected to ground for best thermal performance, however they can be used as routing channels if required.)
15	LIM	I	Selects mode of Digital Output Clipper or AGC
16	AVDD	P	Power supply for internal analog circuitry
17	PVDDB	P	Power Supply for internal power circuitry of Channel B
18	PVDDB	P	
19	BSB+	BST	Connection point for the OUTB+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTB+
20	OUTB+	O	Positive pin for differential speaker amplifier output B
21	OUTB-	O	Negative pin for differential speaker amplifier output B
22	BSB-	BST	Connection point for the OUTB- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTB-
23	PGND	G	Ground for power device circuitry (NOTE: This terminal should be connected to the system ground)
24	BSA-	BST	Connection point for the OUTA- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTA-
25	OUTA-	O	Negative pin for differential speaker amplifier output A
26	OUTA+	O	Positive pin for differential speaker amplifier output A
27	BSA+	BST	Connection point for the OUTA+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTA
28	PVDDA	P	Power Supply for internal power circuitry of Channel A
29	PVDDA	P	
30	PVDDA	P	
31	GGND	G	Ground for gate drive circuitry (this terminal should be connected to the system ground)
32	GVDD	O	Voltage regulator derived from PVDD supply (NOTE: This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
33	SFT_CLIP	I	Sets the maximum output voltage before clipping (Limiter Level)
34	ANA_REG	P	Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry)
35	VCOM	P	Bias voltage for internal PWM conversion block
36	ANA_REF	P	Connection point for internal reference used by ANA_REG and VCOM filter capacitors. And connect to system GND net.
/	EP	G	Provides both electrical and thermal connection from the device to the board. A matching ground pad must be provided on the PCB and the device connected to it via solder. For proper electrical operation, this ground pad must be connected to the system ground.

*1: I: Input; O: Output; G: Ground; P: Power; BST: BOOT Strap

■ ORDERING INFORMATION

Part Number	Package Type	Marking	Operating Temperature Range	Shipping Package MOQ
HT560SQR	QFN36L	HT560SQ XXXXXXXX[1]	-25℃～85℃	Tape and Reel 2500PCS

[1] Production track code.

■ SPECIFICATIONS *1

● Absolute Maximum Ratings *2

PARAMETER	Symbol	MIN	MAX	UNIT
Power supply voltage for AVDD	AVDD	-0.3	30	V
Power supply voltage for PVDD	PVDD	-0.3	30	V
Power supply voltage for DVDD	DVDD	-0.3	4	V
DVDD Referenced Digital Input Voltages	V_I	−0.3	DVDD+0.3	V
Analog Input Voltage (SFT_CLIP, LIM)	V_I	−0.3	GVDD	V
Ambient Operating Temperature	T_A	-25	85	℃
Junction Temperature	T_J	-40	125	℃
Storage Temperature	T_{STG}	-40	125	℃

● Recommended Operating Conditions

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage for AVDD	AVDD		4.5		26	V
Power supply voltage for PVDD	PVDD		4.5		26	V
Power supply voltage for DVDD	DVDD		2.8	3.3	3.63	
Ambient Operating Temperature	T_a		-25	25	85	℃
DVDD Referenced Digital Input Voltages	V_I		0		DVDD	V
Analog Input Voltage (SFT_CLIP, LIM)	V_I		0		GVDD	V
Minimum Speaker Load in BTL Mode	R_L		4			Ω
Minimum Speaker Load in PBTL Mode	R_L		2			Ω

● I/O pins

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Input Logic High threshold for DVDD referenced digital inputs	V_{IH1}	All Digital I/O pins including \FAULT, \SD, FREQ/SDA, PBTL/SCL. PBTL/SCL, GAIN0, GAIN1, SLLEP/ADR, MCLK, SCLK, SDIN, LRCK	70			%DVDD
Input Logic LOW threshold for DVDD Referenced Digital Inputs	V_{IL1}				30	%DVDD
Input Logic HIGH Current Level	I_{IH1}				15	uA
Input Logic LOW Current Level	I_{IL1}				-15	uA
Output Logic LOW Voltage Level	V_{OH}		90			%DVDD
Output Logic LOW Voltage Level	V_{OL}				10	%DVDD
Analog Input Voltage	V_I	SFT_CLIP, LIM	0		GVDD	V

● Master Clock

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable MCLK Duty Cycle	D_{MCLK}		45	50	55	%
Supported MCLK Frequencies	f_{MCLK}	Values include: 128, 192, 256, 384, 512.	128		512	f_s

● Serial Audio Port

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable SCLK Duty Cycle	D_{SCLK}		45	50	55	%
Required LRCK to SCLK Rising Edge			15			ns
Required SDIN Hold Time after SCLK, Rising Edge	t_{HLD}		15			ns
Required SDIN Setup Time before SCLK Rising Edge	t_{su}		15			ns
Supported Input Sample Rates	f_s		32		96	kHz
Supported SCLK Frequencies	F_{sCLK}	Values include: 32, 48, 64	32		64	f_s

*1: Depending on parts and PCB layout, characteristics may be changed.
*2: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Protection Circuitry

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
PVDD Overvoltage Error Threshold	OVE_{RTH}	PVDD Rising		28		V
PVDD Overvoltage Error Threshold	OVE_{FTH}	PVDD Falling		27		V
PVDD Undervoltage Error Threshold	UVE_{RTH}	PVDD Falling		4.2		V
PVDD Undervoltage Error Threshold	UVE_{FTH}	PVDD Rising		4.4		V
Overtemperature Error Threshold	OTE_{TH}			150		℃
Overtemperature Error Hysteresis	OTE_{HYS}			15		℃
Thermal foldback trig point	TFB			135		℃
Thermal Foldback Attack Time	t_{A_TFB}			1200		ms/dB
Thermal Foldback Release Time	t_{A_TFB}			2400		ms/dB
Overcurrent Error Threshold for each BTL Output	OCE_{TH}			10		A
DC Error Threshold	DCE_{TH}			2.6		V
Speaker Amplifier Fault Time Out period	T_{fault}	DCE		650		ms
		DCE or OCP		1.3		s

Speaker Amplifier in All Modes

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 00	AV_{00}			25.2		dBV
Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 01	AV_{01}			28.6		dBV
Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 10	AV_{10}			31		dBV
Speaker Amplifier Gain with SPK_GAIN[1:0] Pins =11	AV_{11}		(Set via I²C)			
Speaker Amplifier DC Offset	$\lvert V_{OS} \rvert$	BTL			10	mV
		PBTL			15	mV
Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 1	$f_{SPK\_AMP(1)}$			16		f_S
Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 0	$f_{SPK\_AMP(0)}$			8		f_S
On Resistance of Output MOSFET (both high-side and low-side)	$R_{DS(ON)}$			120		mΩ
–3-dB Corner Frequency of High-Pass Filter	f_C	f_S = 44.1 kHz		3.7		Hz
		f_S = 48 kHz		4		Hz
		f_S = 88.2 kHz		7.4		Hz
		f_S = 96 kHz		8		Hz

- **Speaker Amplifier in Stereo Bridge Tied Load (BTL) Mode**

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V_N	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, A-Weighted		74		μVrms
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8 Ω, A-Weighted		140		μVrms
Signal to Noise Ratio (Referenced to THD+N=1%)	SNR	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, A-Weighted		98		dB
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8 Ω, A-Weighted		100		dB
Maximum Instantaneous Output Power Per. Ch.	Po	PVDD = 12 V, R_{SPK} = 4 Ω, THD+N = 1%		15		W
		PVDD = 12 V, R_{SPK} = 8 Ω, THD+N = 1%		8.4		W
		PVDD = 15 V, R_{SPK} = 4 Ω, THD+N = 1%		22.5		W
		PVDD = 15 V, R_{SPK} = 8 Ω, THD+N = 1%		13		W
		PVDD = 18 V, R_{SPK} = 4 Ω, THD+N = 1%		25		W
		PVDD = 18 V, R_{SPK} =8 Ω, THD+N = 1%		18.5		W
		PVDD = 24 V, R_{SPK} = 4 Ω, THD+N = 1%		-		W
		PVDD = 24 V, R_{SPK} = 8 Ω, THD+N = 1%		32		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R_{SPK} = 4 Ω, Po = 1 W		0.05		%
		PVDD = 12 V, R_{SPK} =8 Ω, Po = 1 W		0.03		%
		PVDD = 15 V, R_{SPK} = 4 Ω, Po = 1 W		0.05		%
		PVDD = 15 V, R_{SPK} = 8 Ω, Po = 1 W		0.025		%
		PVDD = 18 V, R_{SPK} = 4 Ω, Po = 1 W		0.045		%
		PVDD = 18 V, R_{SPK} = 8 Ω, Po = 1 W		0.02		%
		PVDD = 24 V, R_{SPK} = 4 Ω, Po = 1 W		0.04		%
		PVDD = 24 V, R_{SPK} = 8 Ω, Po = 1 W		0.02		%
Cross-talk (worst case between LtoR and RtoL coupling)	X-Talk	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1kHz Sine		-92		dB
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1kHz Sine		-93		dB

- **Speaker Amplifier in Mono Parallel Bridge Tied Load (PBTL) Mode**

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V_N	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, A-Weighted		75		μVrms
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8 Ω, A-Weighted		140		μVrms
Signal to Noise Ratio (Referenced to THD+N =1%)	SNR	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, A-Weighted		99		dB
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8 Ω, A-Weighted		100		dB
Maximum Instantaneous Output Power.	Po	PVDD = 12 V, R_{SPK} = 4 Ω, THD+N = 1%		16.5		W
		PVDD = 12 V, R_{SPK} = 8 Ω, THD+N = 1%		8.8		W
		PVDD = 15 V, R_{SPK} = 4 Ω, THD+N = 1%		25.7		W
		PVDD = 15 V, R_{SPK} = 8 Ω, THD+N = 1%		13.8		W
		PVDD = 18 V, R_{SPK} = 4 Ω, THD+N = 1%		36.9		W
		PVDD = 18 V, R_{SPK} = 8 Ω, THD+N = 1%		19.7		W
		PVDD = 24 V, R_{SPK} = 4 Ω, THD+N = 1%		64		W
		PVDD = 24 V, R_{SPK} = 8 Ω, THD+N = 1%		34.8		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R_{SPK} = 4 Ω, Po = 1 W		0.036		%
		PVDD = 12 V, R_{SPK} = 8 Ω, Po = 1 W		0.018		%
		PVDD = 15 V, R_{SPK} = 4 Ω, Po = 1 W		0.035		%
		PVDD = 15 V, R_{SPK} = 8 Ω, Po = 1 W		0.017		%
		PVDD = 18 V, R_{SPK} = 4 Ω, Po = 1 W		0.035		%
		PVDD = 18 V, R_{SPK} = 8 Ω, Po = 1 W		0.017		%
		PVDD = 24 V, R_{SPK} = 4 Ω, Po = 1 W		0.034		%
		PVDD = 24 V, R_{SPK} = 8 Ω, Po = 1 W		0.017		%

- **I²C Control Port**

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable Load Capacitance for Each I²C Line	CL(I²C)				400	pF
Support SCL frequency	f_{SCL}				400	kHz
Bus Free time between STOP and START conditions	tbuf		1.3			us
Rise Time, SCL and SDA	tf(I²C)				300	ns
Hold Time, SCL to SDA	th1(I²C)		0			ns
Hold Time, START condition to SCL	th2(I²C)		0.6			us
I²C Startup Time	tI²C(start)				12	ms
Rise Time, SCL and SDA	tr(I²C)				300	ns
Setup Time, SDA to SCL	tsu1(I²C)		100			ns
Setup Time, SCL to START condition	tsu2(I²C)		0.6			us
Setup Time, SCL to STOP condition	tsu3(I²C)		0.6			us
Required Pulse Duration, SCL HIGH	Tw(H)		0.6			us
Required Pulse Duration, SCL LOW	Tw(L)		1.3			us

- **Typical current consumption**

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Quiescent current in DVDD	I_{DVDD}			2.9		mA
DVDD current consumption in sleep mode	I_{DVDD_SLEEP}	SLEEP = H		0.47		mA
DVDD current consumption in SD mode	I_{DVDD_SD}	\SD = L		45		uA

■ TYPICAL OPERATING CHARACTERISTICS

T_A = 25°C, **BTL mode**, f_{SPK_AMP} = 384 kHz, f_{IN} = 1 kHz, unless otherwise noted. Output filter is used as 15 µH and 0.68 µF, unless otherwise noted.

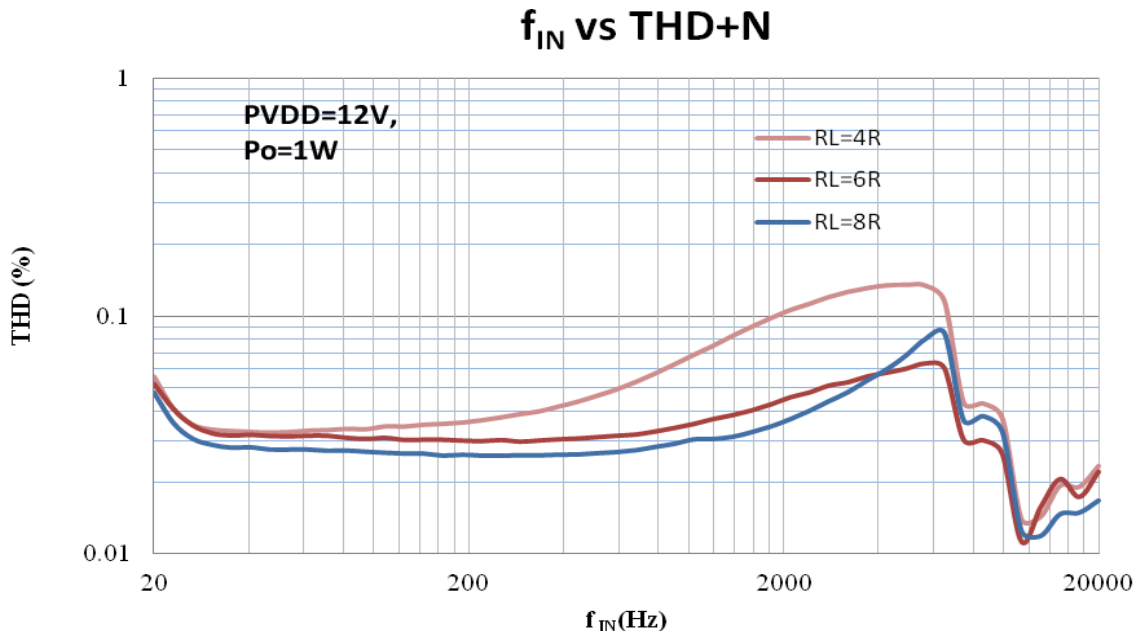


Figure 1. Frequency vs THD+N

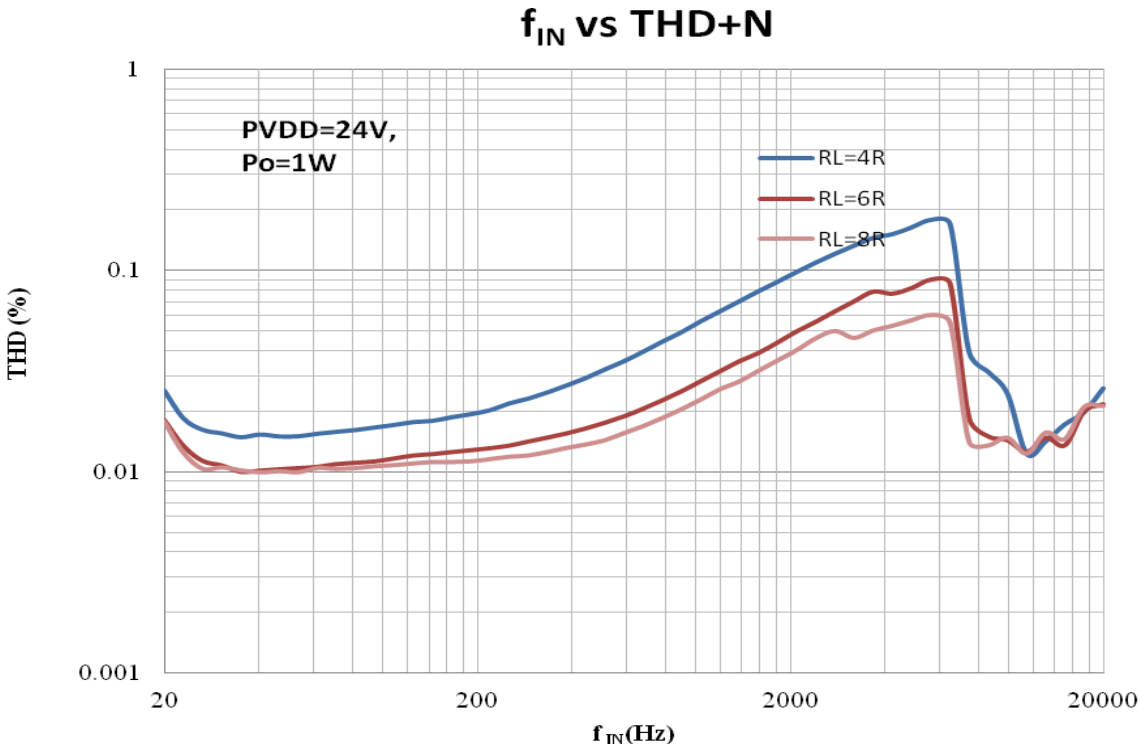


Figure 2. Frequency vs THD+N

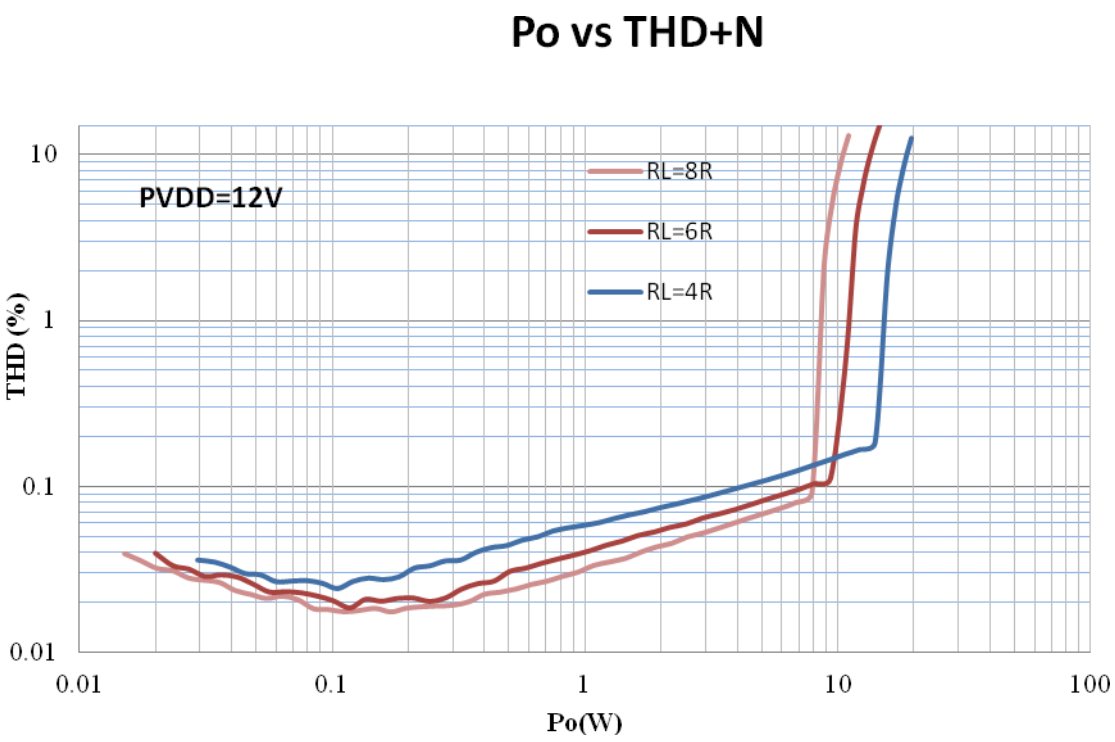


Figure 3. Output Power vs THD+N

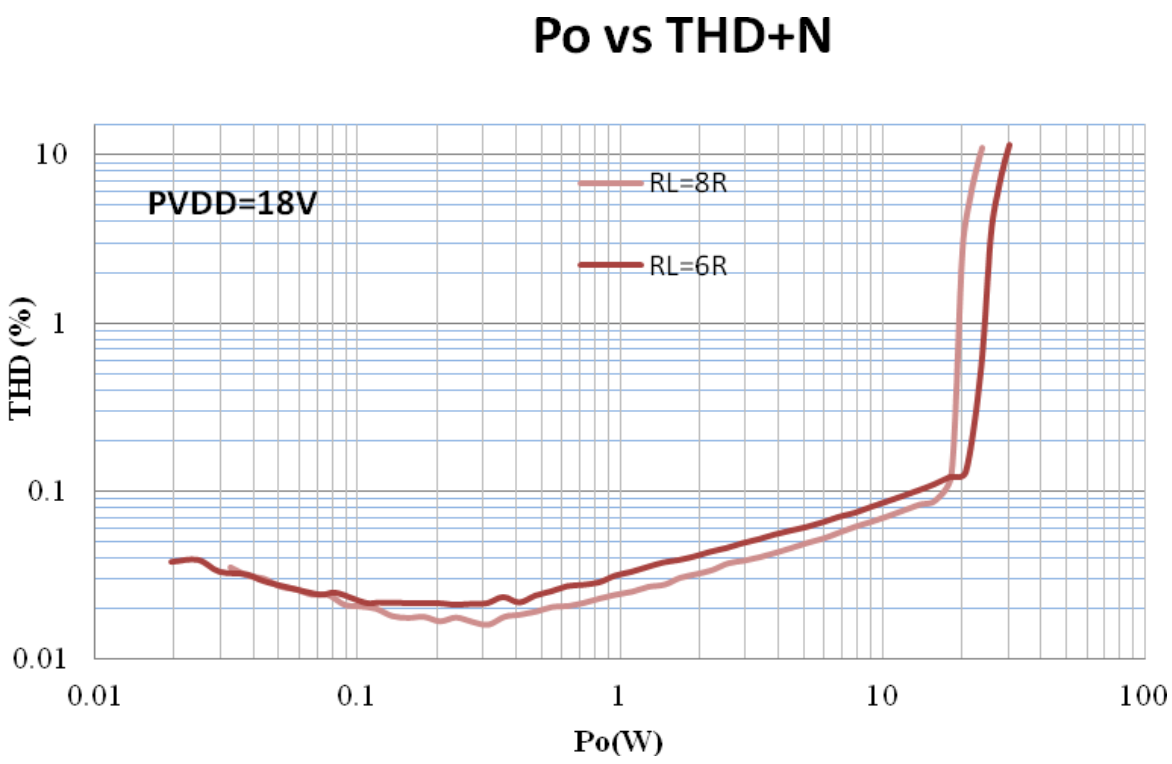


Figure 4. Output Power vs THD+N

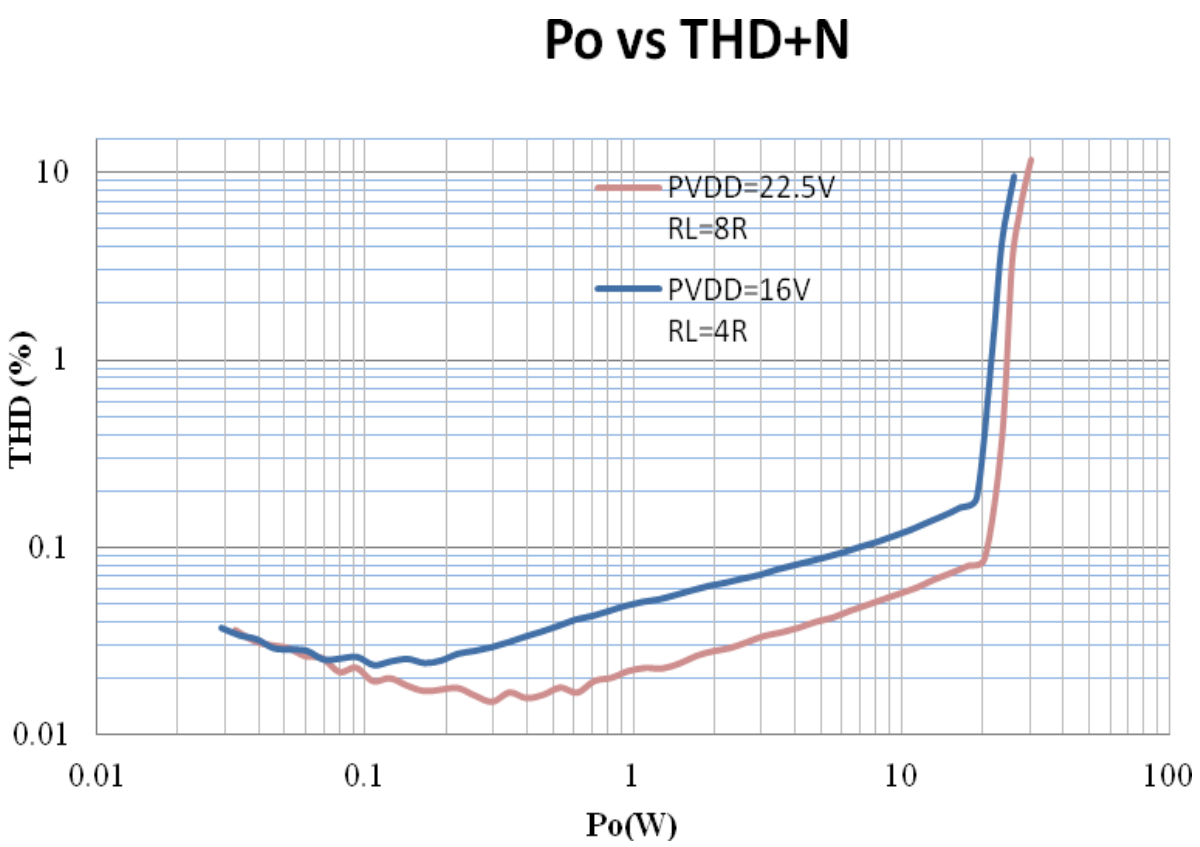


Figure 5. Output Power vs THD+N

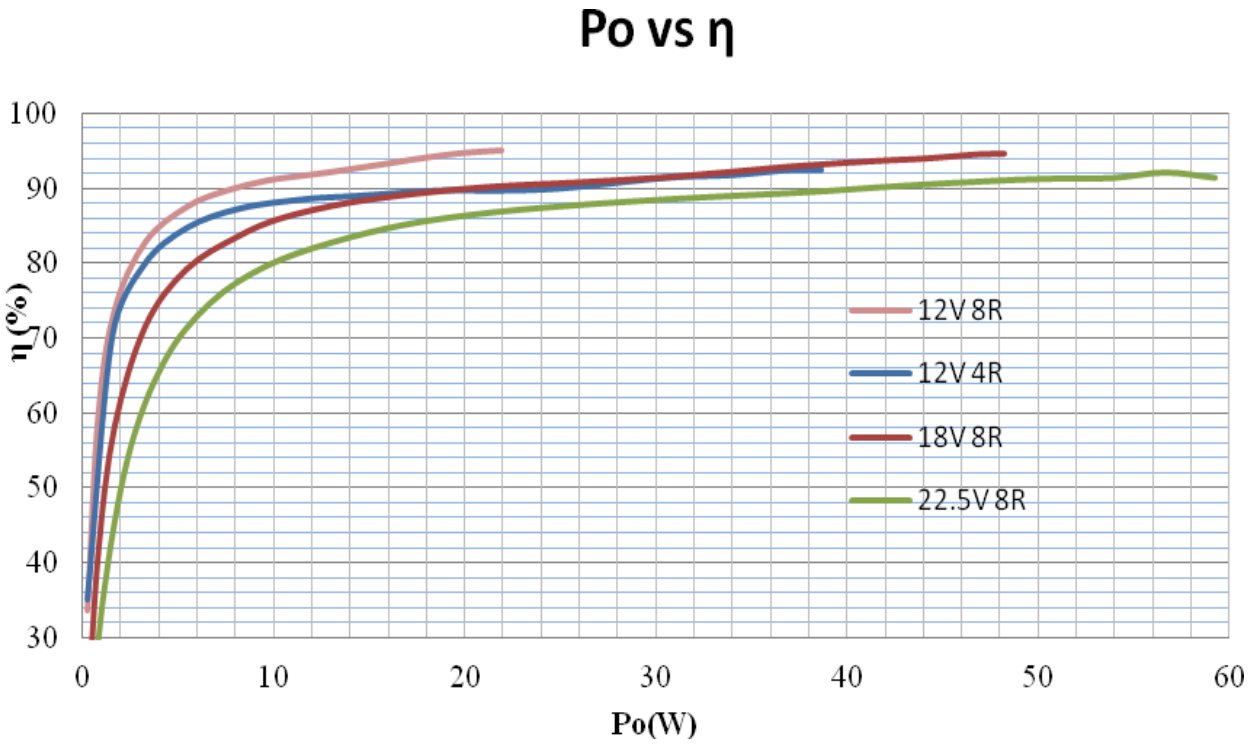


Figure 6. Output Power vs Efficiency

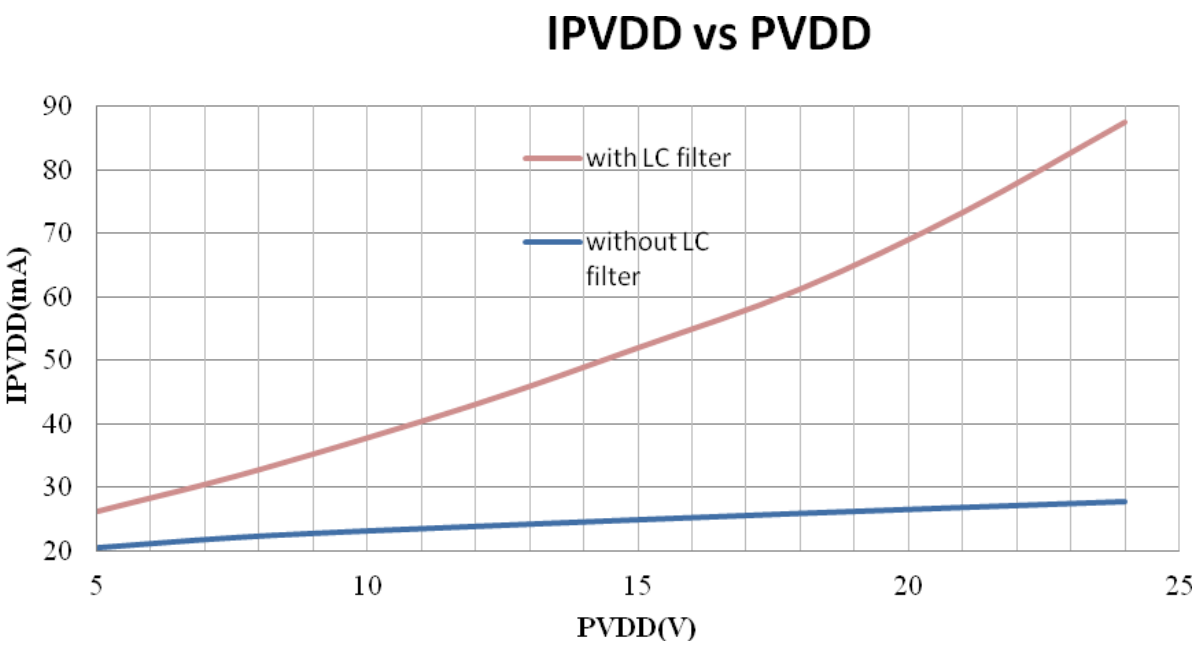


Figure 7. Idle PVDD Current vs PVDD

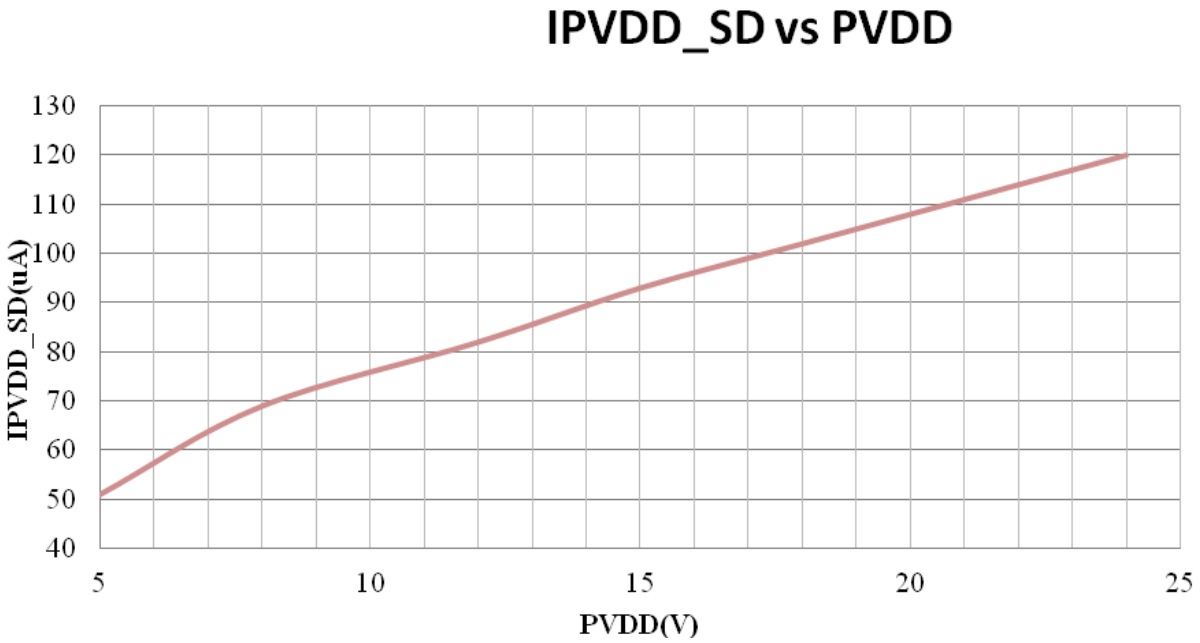


Figure 8. Shutdown PVDD Current vs PVDD

T_A = 25°C, **PBTL mode**, f_{SPK_AMP} = 384 kHz, f_{IN} = 1 kHz, unless otherwise noted. Output filter is used as 15 μH and 0.68 μF, unless otherwise noted.

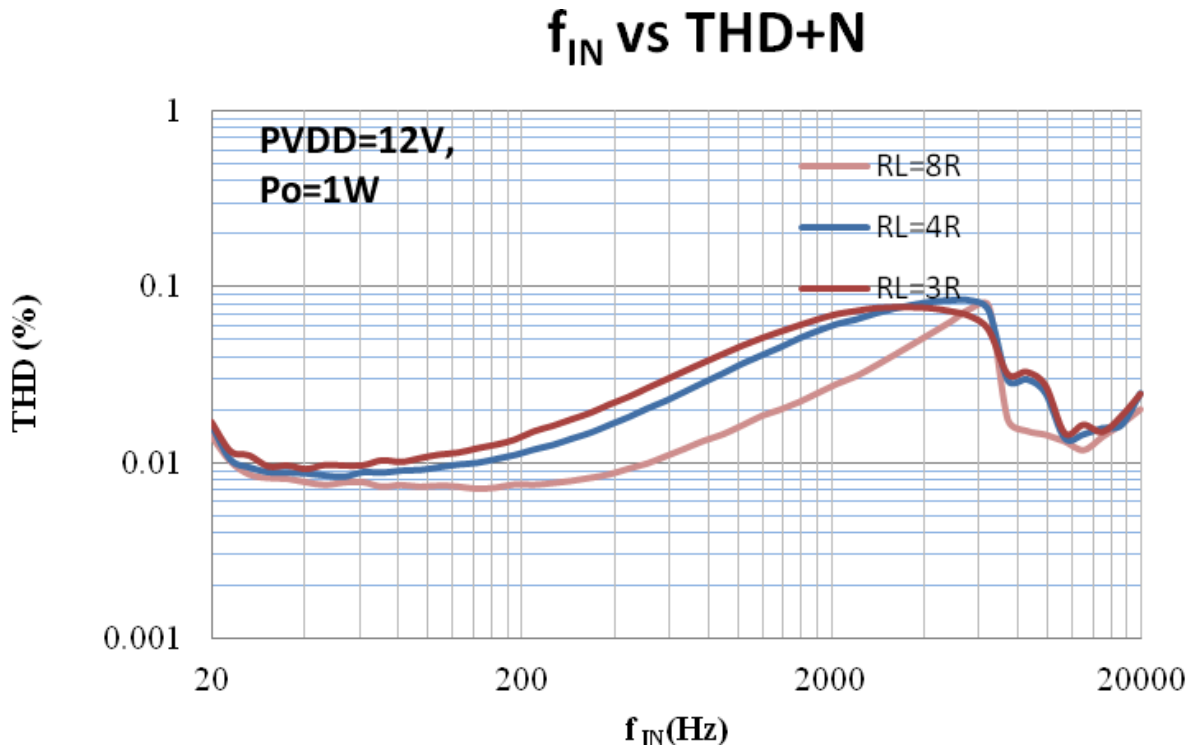


Figure 9. Frequency vs THD+N

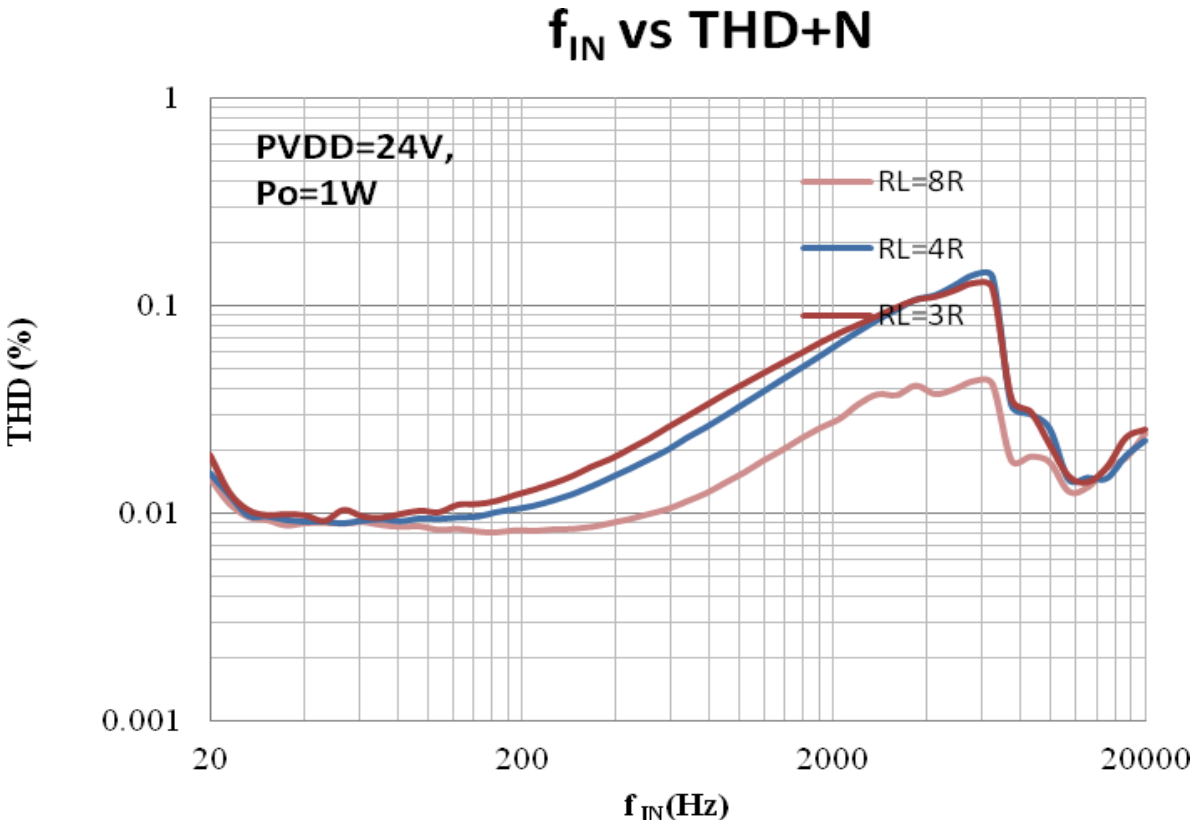


Figure 10. Frequency vs THD+N

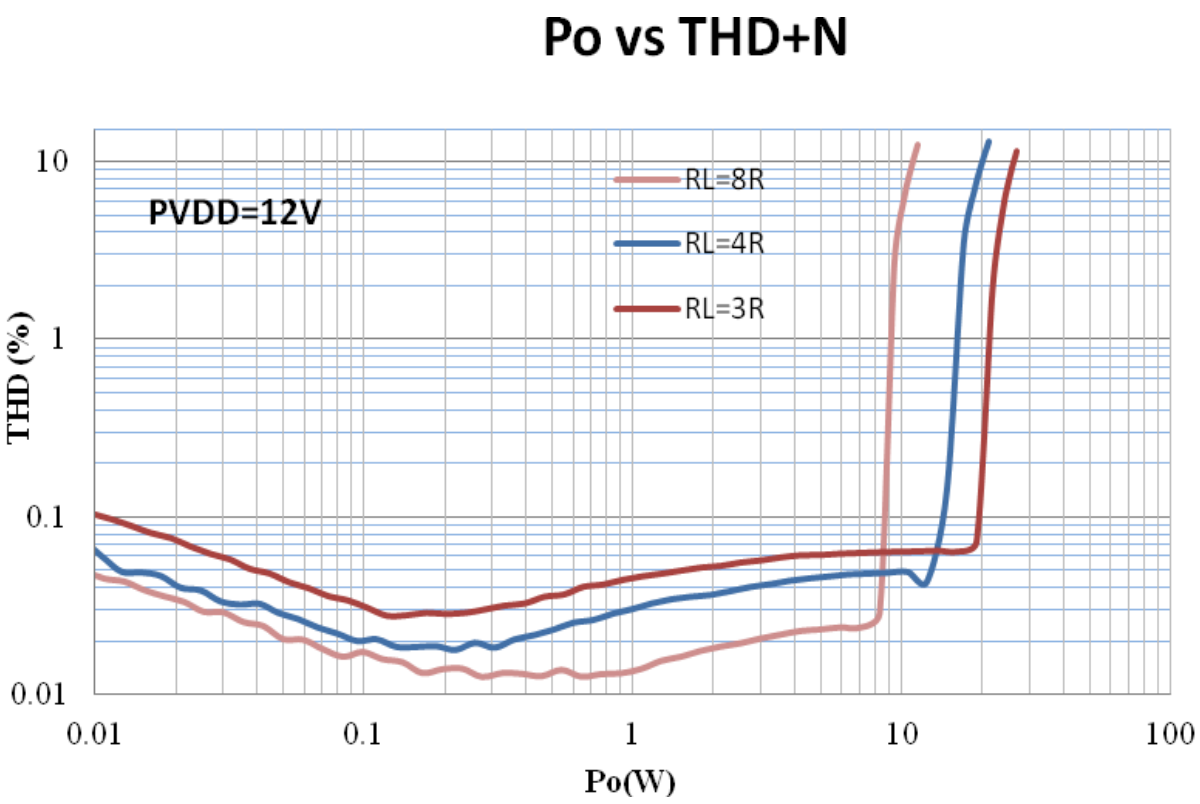


Figure 11. Output Power vs THD+N

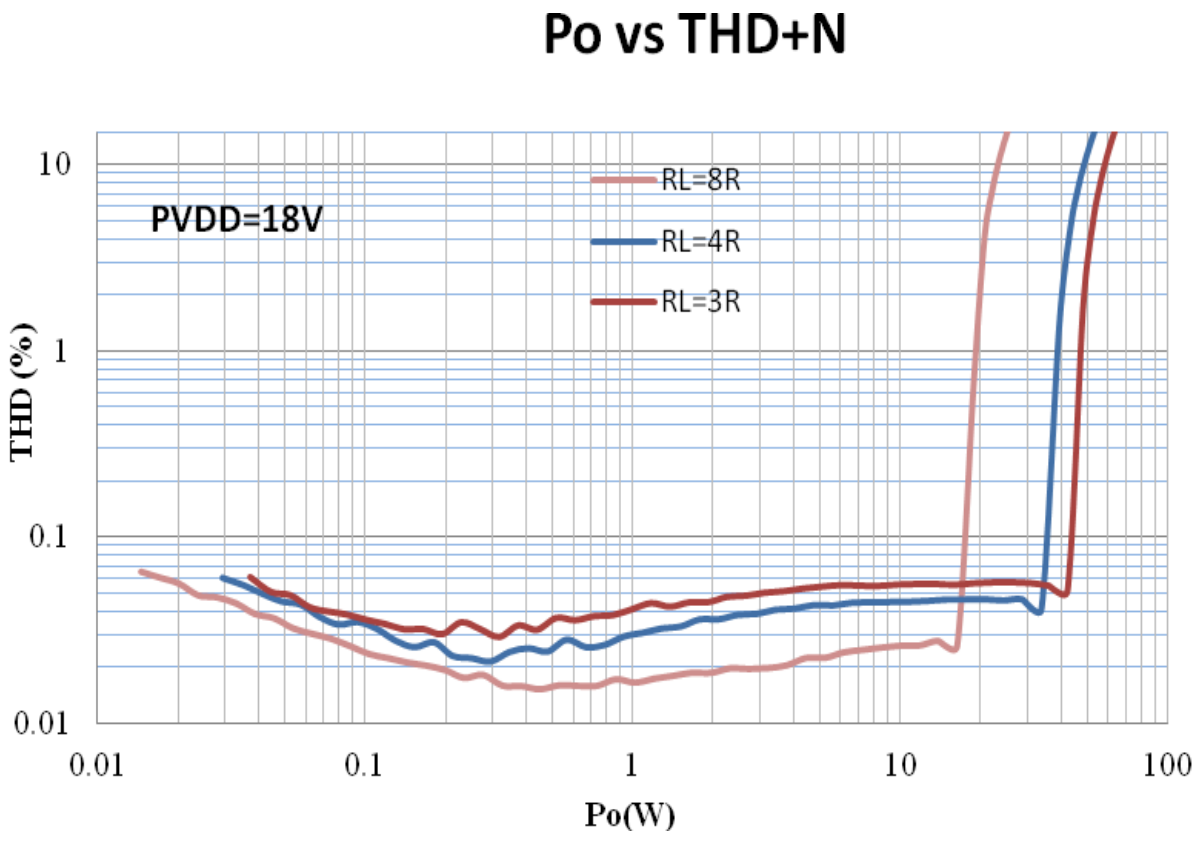


Figure 12. Output Power vs THD+N

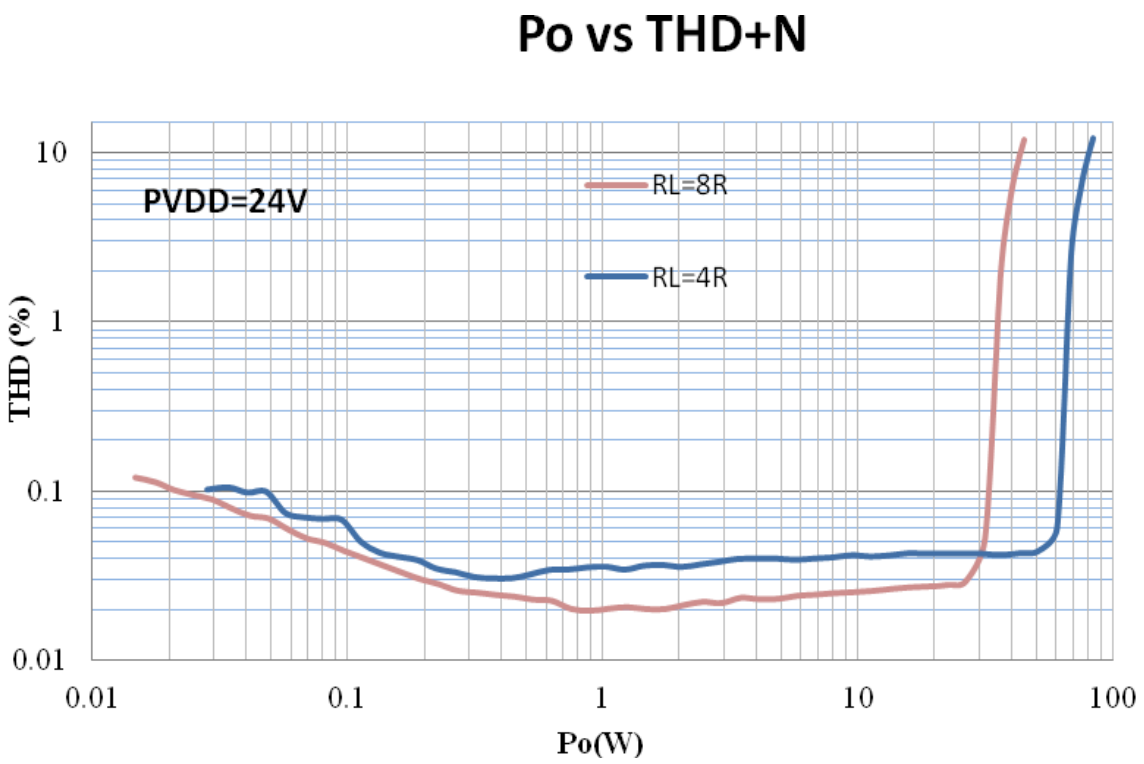


Figure 13. Output Power vs THD+N

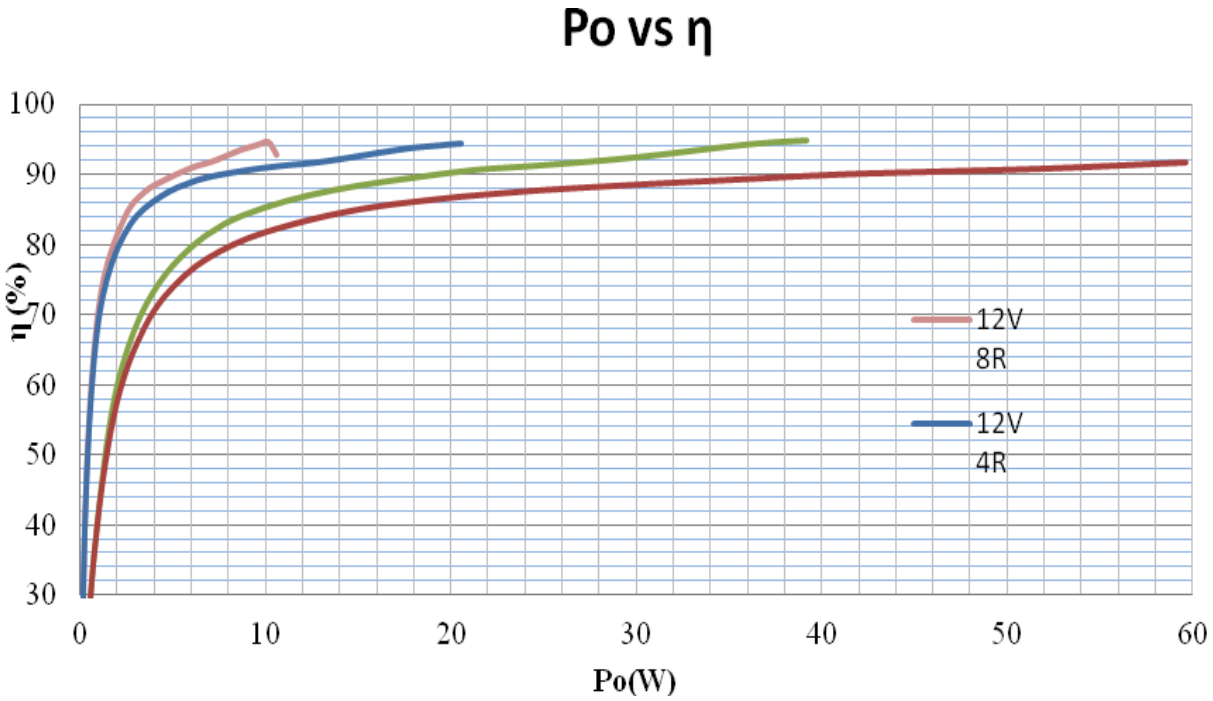


Figure 14. Output Power vs Efficiency

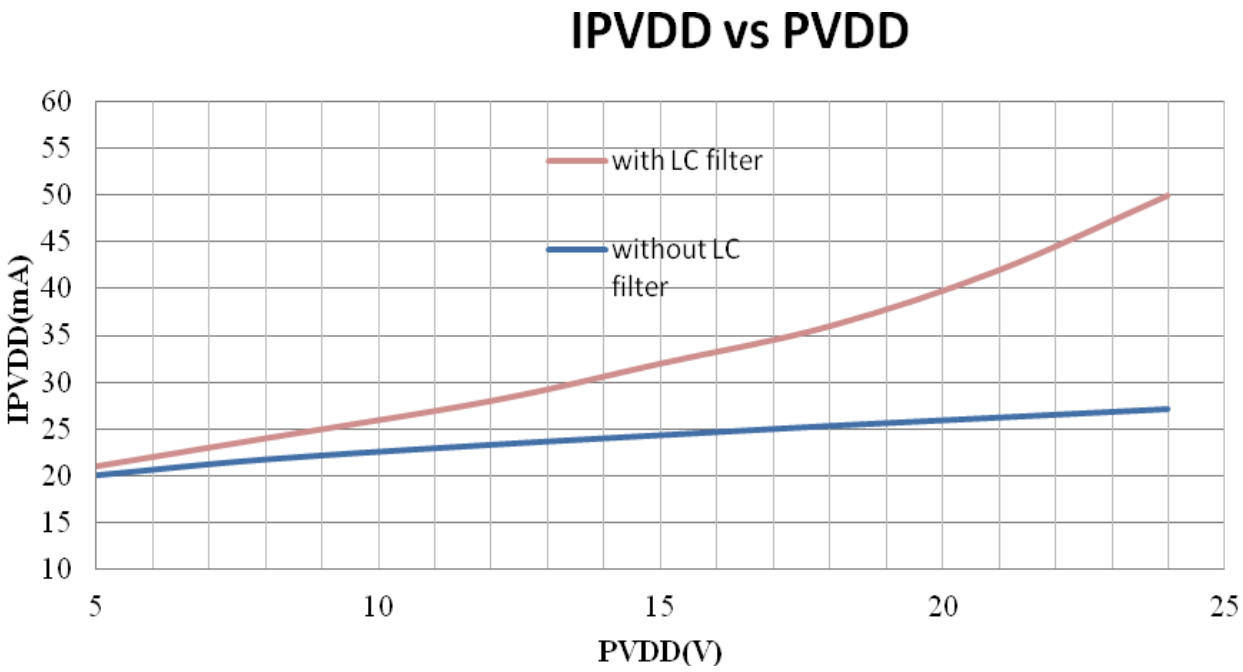


Figure15. Idle PVDD Current vs PVDD

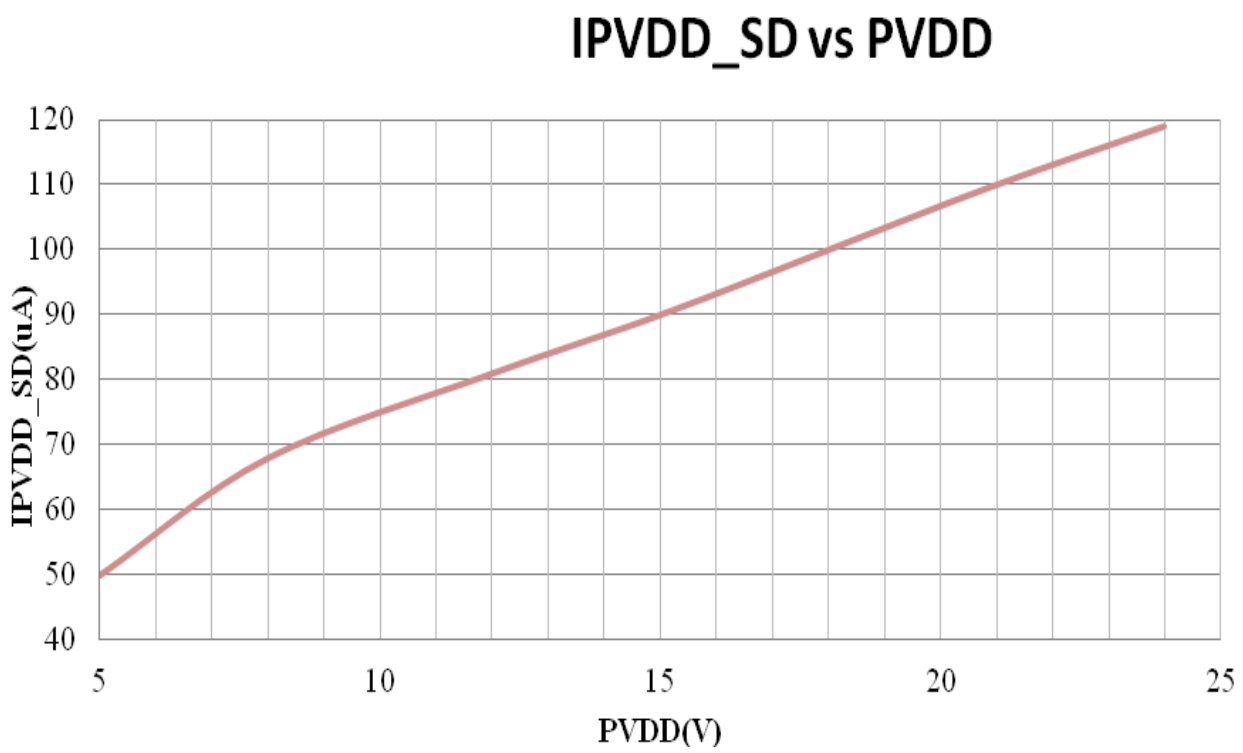


Figure 16. Shutdown PVDD Current vs PVDD

■ APPLICATION INFORMATION

The HT560 is a flexible and easy-to-use stereo class-D speaker amplifier with an I²S input serial audio port. The HT560 supports a variety of audio clock configurations via two speed modes. In Hardware Control mode, the device only operates in single-speed mode. When used in I²C Control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2 kHz and 96 kHz. The outputs of the HT560 can be configured to drive two speakers in stereo Bridge Tied Load (BTL) mode or a single speaker in Parallel Bridge Tied Load (PBTL) mode.

Only two power supplies are required for the HT560. They are a 3.3-V power supply, called VDD, for the small signal analog and digital and a higher voltage power supply, called PVDD for the output stage of the speaker amplifier and AVDD for analog power supply. To enable use in a variety of applications, PVDD can be operated over a large range of voltages, which is 4.5V – 26V, and it is recommended to put paralleled capacitor of 100nF//1uF//220uF between each channel of PVDD and system ground.

1. Speaker Amplifier Audio Signal Path

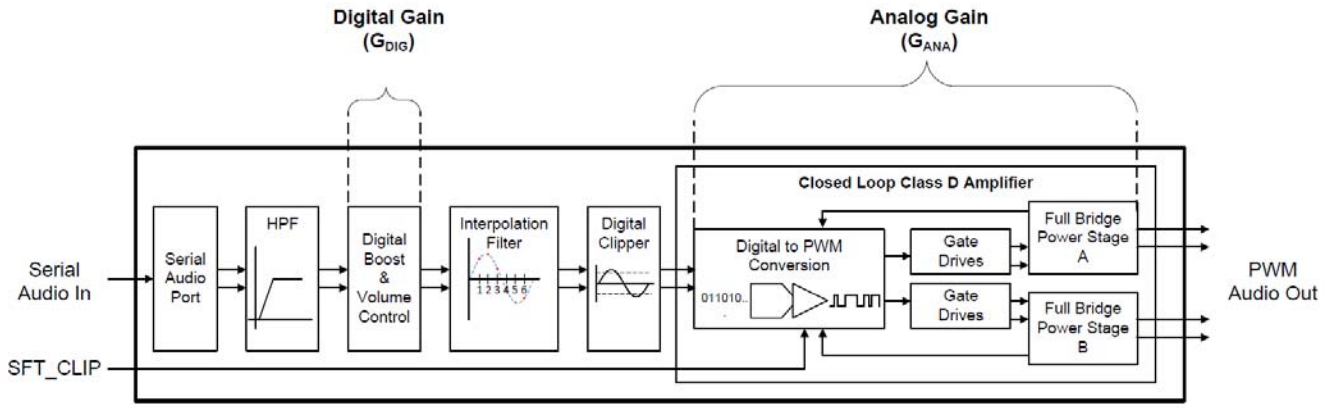


Figure 1 Speaker Amplifier Audio Signal Path

1.1. Serial Audio Port (SAP)

The serial audio port (SAP) receives audio in either I²S, Left Justified, or Right Justified formats. In Hardware Control mode, the device operates only in 32, 48 or 64 × f_S I²S mode. In I²C Control mode, additional options for left-justified and right justified audio formats are available. The supported clock rates and ratios for Hardware Control Mode and I²C Control Mode are detailed in their respective sections below.

1.1.1. I²S

I²S timing uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is LOW for the left channel and HIGH for the right channel. A bit clock, called SCLK, runs at 32, 48, or 64 × f_S and is used to clock in the data. There is a delay of one-bit clock from the time the LRCK signal changes state to the first bit of data on the data lines. The data is presented in 2's-complement form (MSB-first) and is valid on the rising edge of bit clock.

1.1.2. Left-Justified

Left-justified (LJ) timing also uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is HIGH for the left channel and LOW for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCK toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. The HT560 can accept digital words from 16 to 24 bits wide and pads any unused trailing data-bit positions in the L/R frame with zeros before presenting the digital word to the audio signal path.

1.1.3. Right-Justified

Right-justified (RJ) timing also uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is HIGH for the left channel and LOW for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCK transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The HT560 pads unused leading data-bit positions in the left/right frame with zeros before presenting the digital word to the audio signal path.

1.2. DC Blocking Filter

Excessive DC content in the audio signal can damage loudspeakers and even small amounts of DC offset in the signal path cause audible artifacts when muting and unmuting the speaker amplifier. For these reasons, the amplifier employs two separate DC blocking methods for the speaker amplifier. The first is a high-pass filter provided at the front of the data path to remove any DC from incoming audio data before it is presented to the audio path. The –3 dB corner frequencies for the filter are specified in the speaker amplifier electrical characteristics table. In Hardware Control mode, the DC blocking filter is active and cannot be disabled. In I²C Control mode, the filter can be bypassed by writing a 1 to bit 6 of register 0x15. The second method is a DC detection circuit that will shut down the power stage and issue a latching fault if DC is found to be present on the output due to some internal error of the device. This DC Error (DCE) protection is discussed in the Protection Circuitry section below.

1.3. Digital Boost and Volume Control

Following the high-pass filter, a digital boost block is included to provide additional digital gain if required for a given application as well as to set an appropriate clipping point for a given GAIN[1:0] pin configuration when in Hardware Control mode. The digital boost block defaults to +6dB when the device is in Hardware Mode. In most use cases, the digital boost block will remain unchanged when operating the device in I²C Control mode, as the volume control offers sufficient digital gain for most applications. The HT560's digital volume control operates from Mute to 24 dB, in steps of 0.5 dB. The equation below illustrates how to set the 8-bit volume control register at address 0x13/0x14:

DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB])

Transitions between volume settings will occur at a rate of 0.5 dB every 8 LRCK cycles to ensure no audible artifacts occur during volume changes. This volume fade feature can be disabled via Bit 7 of Register 0x15.

1.4. Digital Clipper

A digital clipper is integrated in the oversampled domain to provide a component-free method to set the clip point of the speaker amplifier. Through the "Digital Clipper Level x" (at register address 0x10, 0x11, 0x12) controls in the I²C control port, the point at which the oversampled digital path clips can be set directly, which in turns sets the 10% THD+N operating point of the amplifier. This is useful for applications in which a single system is designed for use in several end applications that have different power rating specifications. Its place in the oversampled domain ensures that the digital clipper is acoustically appealing and reduces or eliminates tones which would otherwise foldback into the audio band during clipping events. Figure 2 shows a block diagram of the digital clipper.

The audio signature of the amplifier when the digital clipper is active is very smooth, owing to its place in the signal chain.

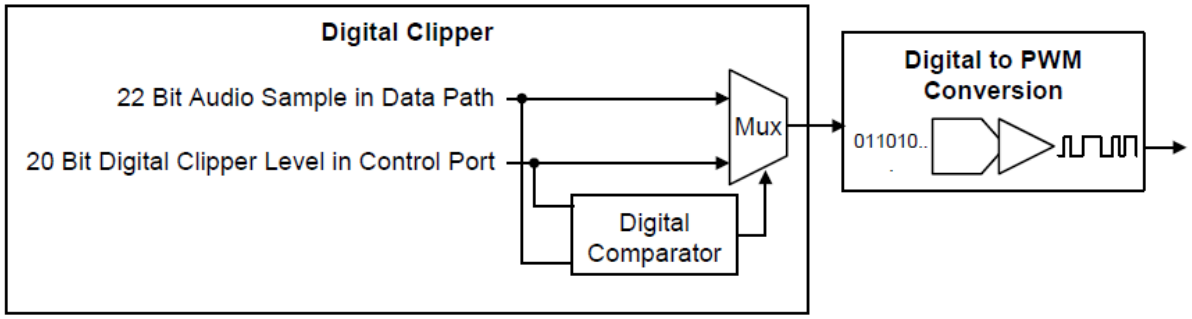


Figure 2 Digital Clipper Simplified Block Diagram

It is important to note that the actual signal developed across the speaker will be determined not only by the digital clipper, but also the analog gain of the amplifier. Depending on the analog gain settings and the PVDD level applied, clipping could occur as a result of the voltage swing that is determined by the gain being larger than the available PVDD supply rail. The gain structures are discussed in detail below for both Hardware Control Mode and I²C Control Mode.

1.5. Closed-Loop Class-D Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed-Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device. The gain structures are discussed in detail below for both Hardware Control Mode and I²C Control Mode.

The switching rate of the amplifier is configurable in both Hardware Control Mode and I²C Control Mode. In both cases, the PWM switching frequency is a multiple of the sample rate. This behavior is described in the respective Hardware Control Mode and I²C Control Mode sections below.

2. Speaker Amplifier Protection Suite

The speaker amplifier in the HT560 includes a robust suite of error handling and protection features. It is protected against Over-Current, Under-Voltage, Over-Voltage, Over-Temperature, DC, and Clock Errors. The status of these errors is reported via the FAULT pin and the appropriate error status register in the I²C Control Port. The error or handling behavior of the device is characterized as being either "Latching" or "Non-Latching" depending on what is required to clear the fault and resume normal operation (that is playback of audio).

For latching errors, the \SD pin or the SD bit in the control port must be toggled in order to clear the error and resume normal operation. If the error is still present when the \SD pin or SD bit transitions from LOW back to HIGH, the device will again detect the error and enter into a fault state resulting in the error status bit being set in the control port and the \FAULT line being pulled LOW. If the error has been cleared (for example, the temperature of the device has decreased below the error threshold) the device will attempt to resume normal operation after the \SD pin or SD bit is toggled and the required fault time out period (T_{FAULT}) has passed. If the error is still present, the device will once again enter a fault state and must be placed into and brought back out of shutdown in order to attempt to clear the error.

For non-latching errors, the device will automatically resume normal operation (that is playback) once the error has been cleared. The non-latching errors, with the exception of clock errors will not cause the \FAULT line to be pulled LOW. It is not necessary to toggle the \SD pin or SD bit in order to clear the error and resume normal operation for non-latching errors. Table. 1 details the types of errors protected by the HT560's Protection Suite and how each are handled.

Table. 1 Protection Suite Error Handling Summary

ERROR	CAUSE	FAULT TYPE	Error Is Cleared By
Overvoltage Error (OVE)	PVDD level rises above that specified by OVE_{RTH}	Non-latching	PVDD level returning below OVE_{FTH}
Undervoltage Error (UVE)	PVDD level drops below that specified by UVE_{RTH}	Non-latching	PVDD level returning above UVE_{RTH}
Clock Error (CLKE)	One or more of the following errors has occurred: 1. Non-supported MCLK to LRCK and/or SCLK to LRCK Ratio; 2. Non-supported MCLK or LRCK rate 3. MCLK, SCLK, or LRCK has stopped	Non-latching	Clocks returning to valid state
Overcurrent Error (OCE)	Speaker Amplifier output current has	Latching	\FAULT has passed AND

	increased above the level specified by OCE_{TH}		\SD Pin or Bit Toggle
DC Detect Error (DCE)	DC offset voltage on the speaker amplifier output has increased above the level specified by the DCE_{TH}	Latching	\FAULT has passed AND \SD Pin or Bit Toggle
Overtemperature Error (OTE)	The temperature of the die has increased above the level specified by the OTE_{TH}	Latching	\FAULT has passed AND \SD Pin or Bit Toggle AND the temperature of the device has reached a level below that which is dictated by the OTE_{HYS} specification

2.1. \FAULT pin

In both hardware and I²C Control mode, the \AULT pin of the HT560 serves as a fault indicator to notify the system that a fault has occurred with the speaker amplifier by being actively pulled LOW. This pin is an open-drain output pin and, unless one is provided internal to the receiver, requires an external pullup to set the net to a known value. The behavior of this pin varies based upon the type of error which has occurred.

In the case of a latching error, the fault line will remain LOW until such time that the HT560 has resumed normal operation (that is the \SD pin has been toggled and T_{FAULT} has passed).

With the exception of clock errors, non-latching errors will not cause the \FAULT pin to be pulled LOW. Once a non-latching error has been cleared, normal operation will resume. For clocking errors, the \FAULT line will be pulled LOW, but upon clearing of the clock error normal operation will resume automatically, that is, with no T_{FAULT} delay.

One method which can be used to convert a latching error into an auto-recovered, non-latching error is to connect the \FAULT pin to the \SD pin. In this way, a fault condition will automatically toggle the \SD pin when the \FAULT pin goes LOW and returns HIGH after the \FAULT period has passed.

2.2. DC Detect Protection

The HT560 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. The device behavior in response to a DCE event is detailed in the table in the previous section.

A DCE event occurs when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. The table below shows some examples of the typical DCE Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2 Hz.

The minimum output offset voltages required to trigger the DC detect are listed in Table. 2. The outputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

Table. 2 DC Detect Threshold

PVDD (V)	|Vos| (V)
4.5	0.96
6	1.3
12	2.6
18	3.9

2.3. Foldback (TFB) Function

The HT560 Thermal Foldback, TFB, is designed to protect the HT560 from excessive die temperature in case of the device being operated beyond the recommended temperature or power limit, or with a weaker thermal system than recommended, without shutting the device down. In hardware control mode, it's enabled by default. In I²C control mode, the function can be disabled through bit 4 register of 0x00.

The TFB works by reducing the on die power dissipation by reducing the HT560 system gain by the rate of attack

time (default value 1200ms/dB, can be modified in register address 0x00 in I²C control mode) by 0.25dB per step (step pace, which can be modified at bit 6 of register 0x00 in I²C control mode) if the TFB trig point is exceeded. Once the die temperature drops below the TFB trig point, the HT560 gain is increased by a single or by the rate of release time (default value 2400ms/dB, can be modified in register address 0x00 in I²C control mode) by 0.25dB per step (step pace, which can be modified at bit 6 of register 0x00 in I²C control mode) until the TFB trig point, or a maximum attenuation is reached, and the system gain will be decreased again, or the system gain is at its nominal gain level. The procedure shows as follows.

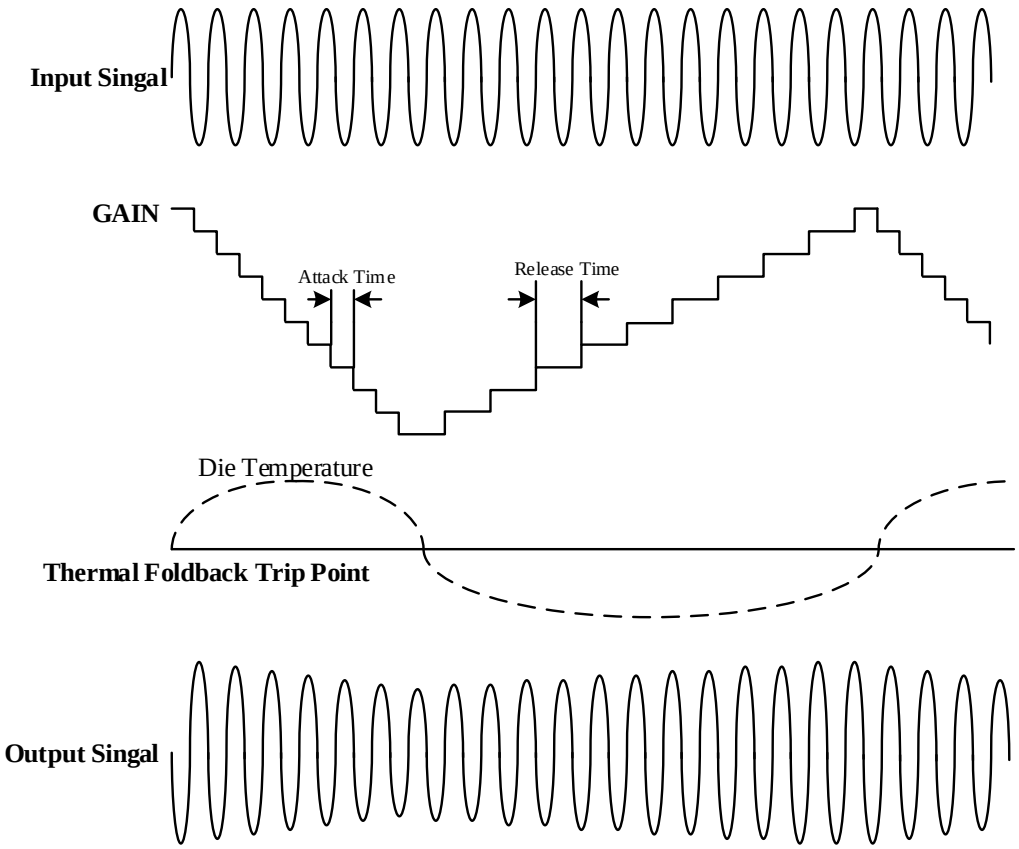


Figure 3 TFB Operation

3. Device Functional Modes

3.1. Hardware Control Mode

For systems which do not require the added flexibility of the I²C control port or do not have an I²C host controller, the HT560 can be used in Hardware Control Mode. In this mode of operation, the device operates in its default configuration and any changes to the device are accomplished via the hardware control pins, described below. The audio performance between Hardware and I²C Control mode is identical, however more features and functionality are available when the device is operated in I²C Control mode. The behavior of these Hardware Control Mode pins is described in the sections below.

Several static I/O's are present on the HT560 which are meant to be configured during PCB design and not changed during normal operation. Some examples of these are the GAIN[1:0] and PBTL/SCL pins. These pins are often referred to as being tied or pulled LOW or tied or pulled HIGH. A pin which is tied or pulled LOW has been connected directly to the system ground. The HT560 is configured such that the most popular use cases for the device (that is BTL mode, 384-kHz switching frequency, and so forth) require the static I/O lines to be tied LOW. This ensures optimum thermal performance as well as BOM reduction.

Device pins that need to be tied or pulled HIGH should be connected to DVDD. For these pins, a pull-up resistor is recommended to limit the slew rate of the voltage which is presented to the pin during power up. Depending on the output impedance of the supply, and the capacitance connected to the DVDD net on the board, slew rates of this node could be high enough to trigger the integrated ESD protection circuitry at high current levels, causing damage to the

device. It is not necessary to have a separate pull-up resistor for each static digital I/O pin.

Instead, a single resistor can be connected to DVDD and all static I/O lines which are to be tied HIGH can be connected to that pull-up resistor. This connectivity is shown in the Typical Application Circuits. These pullup resistors are not required when the digital I/O pins are driven by a controlled driver, such as a digital control line from a systems processor, as the output buffer in the system processor will ensure a controlled slew rate.

3.1.1. Speaker Amplifier Shut Down (\SD pin)

In both Hardware and I²C Control mode, the \SD pin is provided to place the speaker amplifier into shutdown. Driving this pin LOW will place the device into shutdown, while pulling it HIGH (to DVDD) will bring the device out of shutdown. This is the lowest power consumption mode that the device can be placed in while the power supplies are up. If the device is placed into shutdown while in normal operation, an audible artifact may occur on the output. To avoid this, the device should first be placed into sleep mode, by pulling the SLEEP/ADR pin HIGH before pulling the SPK_SD low.

It is recommended that the duration between 2 actions of Shut Down should be more than 10 msec, therefore a capacitor (bigger than 0.1uF) should be connected between \SD pin and the system ground.

3.1.2. Serial Audio Port in Hardware Control Mode

When used in Hardware Control Mode, the Serial Audio Port (SAP) accepts only I²S formatted data. Additionally, the device operates in Single-Speed Mode (SSM), which means that supported sample rates, MCLK rates, and SCLK rates are limited to those shown in the table below. Additional clocking options, including higher sample rates, are available when operating the device in I²C Control Mode.

Table. 3 details the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK rate, the supported SCLK rates are shown and are represented in multiples of the sample rate, which is written as "× f_S".

Table. 3 Supported SCLK rates in hardware control mode (Single speed mode)

Sample Rate fs (kHz)	**MCLK rate (× fs)**				
	128	192	256	384	512
	SCLK rate (× fs)				
12	N/S	N/S	N/S	N/S	32, 48, 64
16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64
24	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
38	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
44.1	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64

3.1.3. Power Limit Function

There are two different power limit functions for HT560, one is Automatic Gain Control (AGC), the other is Power Clipper (PCLP). The function can be selected by setting the LIM pin.

3.1.3.1. Power Limit Mode (LIM pin)

The LIM pin configuration is shown as Figure 4 and Table. 4.

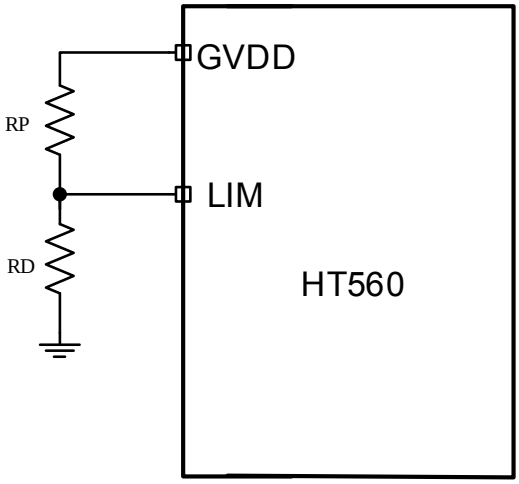


Figure 4 LIM Terminal Configuration

Table. 4 LIM Terminal Settings

Voltage of LIM Terminal	Power Limit Mode	Attack Time T_A (us/dB)	Release Time T_R (ms/dB)
GVDD	AGC FAST	80	400
2/3 GVDD	AGC MEDIUM	160	800
1/3 GVDD	AGC SLOW	320	1600
GND	PCLP	/	

If the AGC function is selected, the output music can be limited below the preset Limiter Level (see pin SFT_CLIP). If the output audio signal exceeds the Limiter Level, HT560 decreases amplifier gain by the rate of attack time by 0.25dB per step (step pace). HT560 increases the gain by the rate release time by 0.25dB/step (step pace) once the output audio is below the limiter level. Figure 5 shows this relationship.

The AGC function can be used both in Hardware and I²C control mode. In Hardware control mode, there are 3 different groups of attack time and release time can be selected by LIM pin, shown as table 4. In I²C control mode, the Power Limit Function is selected at the bit 5 of register 0x00, the attack time and release time of the AGC function is configured at register 0x01, the step pace can be configured at bit 6 of register 0x00.

The AGC function don't clip the output wave while limiting the output power. It can remove the output clipping noise and protect the speakers caused by a reduction of power supply voltage or a sudden large volume of input music.

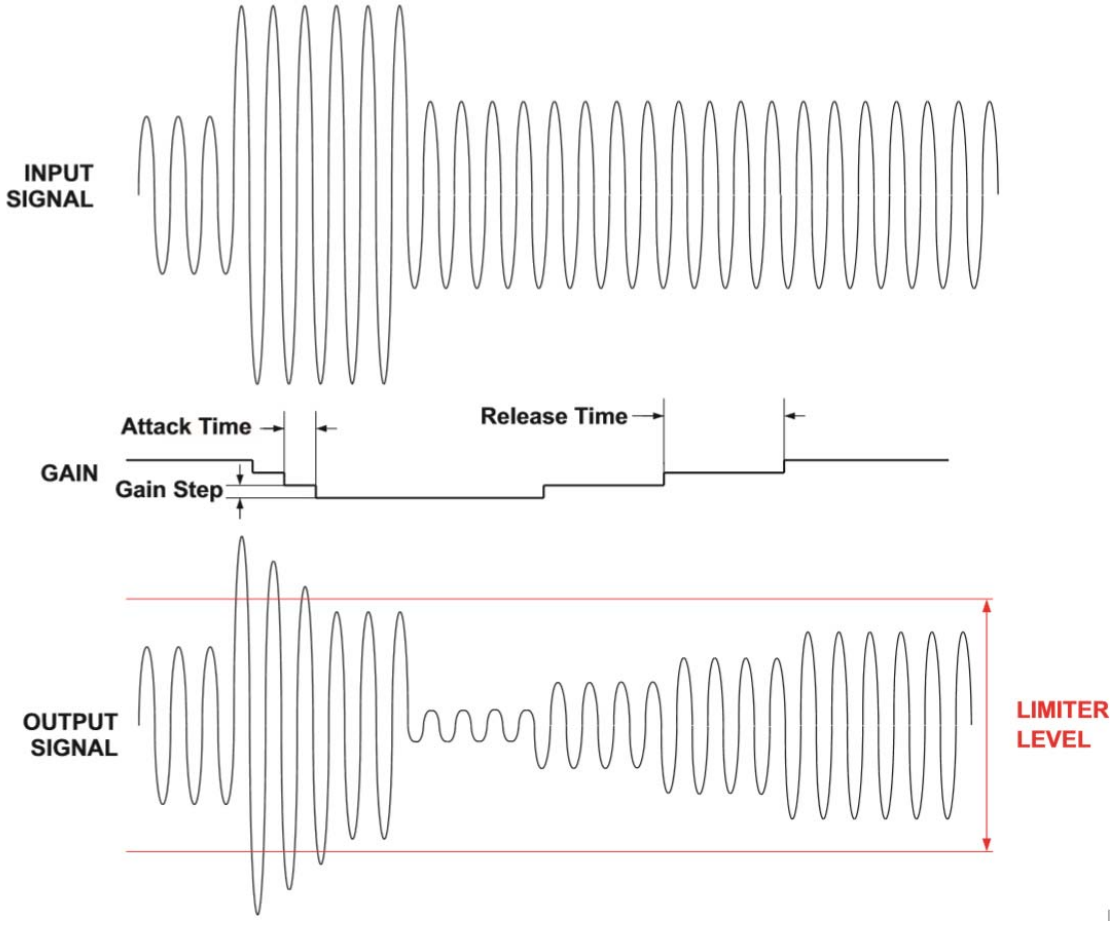


Figure 5 AGC Function Description

The HT560 also has a power clipper function (PLCP) that can be used to clip the output voltage level below the supply rail. The PLCP function can be selected by pulling LIM pin down into system ground, shown as Table. 4.

When PLCP function is active, the amplifier operates as if it was powered by a lower supply voltage, and thereby enters into clipping sooner than if the circuit was not active. The result is clipping behavior very similar to that of clipping at the PVDD rail, in contrast to the digital clipper behavior which occurs in the oversampled domain of the digital path. The point at which clipping begins is called the Limiter Level (see pin SFT_CLIP).

To move the output stage into clipping, the PCLP function limits the duty cycle of the output PWM pulses to a fixed maximum value. After filtering this limit applied to the duty cycle resembles a clipping event at a voltage below that of the PVDD level.

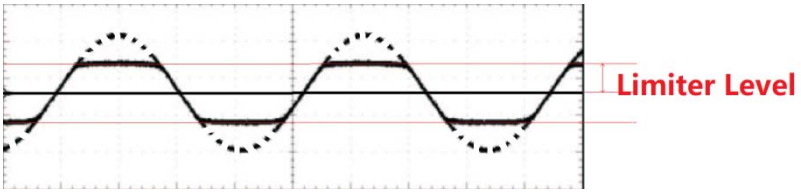


Figure 6 PCLP Function Description

3.1.3.2. Limiter Level Configuration (SFT_CLIP pin)

The Limiter Level is controlled by a resistor divider from GVDD (around 5.5V) to ground, which sets the voltage at the SFT_CLIP pin (V_{SFT_CLIP}). The Limiter Level is approximately 4 times the voltage at the SFT_CLIP pin, noted as V_{SFT_CLIP}.

$$\text{Limiter Level} \approx 4 \times V_{SFT\_CLIP}$$

The precision of the threshold at which clipping occurs is dependent upon the voltage level at the SFT_CLIP pin.

Because of this, increasing the precision of the resistors used to create the voltage divider, or using an external reference will increase the precision of the point at which the device enters into clipping. To ensure stability, and soften the edges of the clipping event, a capacitor should be connected from pin SFT_CLIP to ground.

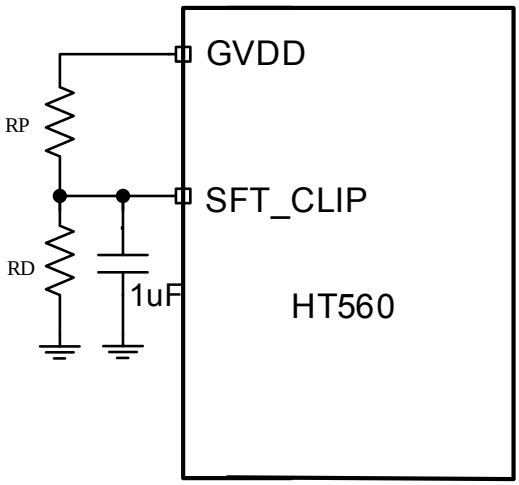


Figure 7 SFT_CLIP Terminal Configuration

If LIM pin is connected to GND, and SFT_CLIP pin is directly connected to GVDD, neither function of AGC nor PCLP is selected.

3.1.4. Speaker Amplifier Switching Frequency Select (FREQ/SDA pin)

In Hardware Control mode, the PWM switching frequency of the HT560 is configurable via the FREQ/SDA pin. When connected to the system ground, the pin sets the output switching frequency to 8 × f_S. When connected to DVDD through a pull-up resistor, as shown in the Typical Application Circuits, the pin sets the output switching frequency to 16 × f_S. More switching frequencies are available when the HT560 is used in I²C Control Mode. Please notice that a switching frequency between 300kHz and 600kHz will get a better performance for the Class D amplifier. For example, an output switching frequency of 8 × f_S is recommended when 48kHz fs is used. Detailed recommendations for the FREQ selection are listed in Table. 8 Recommendations for the FREQ Selection

3.1.5. Parallel Bridge Tied Load Mode Select (PBTL/SCL pin)

The HT560 can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the output impedance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of current the speaker amplifier can source before hitting the over-current error threshold.

The device can be placed operated in PBTL mode in either Hardware Control Mode or in I²C Control Mode.

To place the HT560 into PBTL Mode when operating in Hardware Control Mode, the PBTL/SCL pin should be pulled HIGH (that is, connected to the DVDD supply through a pull-up resistor). If the device is to operate in BTL mode instead, the PBTL/SCL pin should be pulled LOW, that is connected to the system supply ground. When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

In PBTL mode, the amplifier selects its source signal from the right channel of the stereo signal presented on the SDIN line of the Serial Audio Port. To select the right channel of the stereo signal, the LRCK can be inverted in the processor that is sending the serial audio data to the HT560.

3.1.6. Speaker Amplifier Sleep Enable (SLEEP/ADR pin)

In Hardware Control mode, pulling the SLEEP/ADR pin HIGH gracefully transitions the switching of the output devices to a non-switching state or "High-Z" state. This mode of operation is similar to mute in that no audio is present on the outputs of the device. However, unlike the 50/50 mute available in the I²C Control Port, sleep mode saves quiescent power dissipation by stopping the speaker amplifier output transistors from switching. This mode of operation saves quiescent current operation but keeps signal path blocks active so that normal operation can resume more quickly than if the device were placed into shutdown. It is recommended to place the device into sleep mode

before stopping the audio signal coming in on the SDIN line or before bringing down the power supplies connected to the HT560 in order to avoid audible artifacts.

It is recommended that the duration between 2 actions of enabling SLEEP should be more than 10 msec, therefore a capacitor (bigger than 0.1uF) should be connected between SLEEP pin and the system ground.

3.1.7. Speaker Amplifier Gain Select (GAIN[1:0] pin)

In Hardware Control Mode, a combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. The decode of the two pins "GAIN1" and "GAIN0" sets the gain of the speaker amplifier. Additionally, pulling both of the GAIN[1:0] pins HIGH places the device into I2C control mode.

As seen in Figure 8, the audio path of the HT560 consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown as GDIG in the digital audio path and the analog gain from the input of the analog modulator GANA to the output of the speaker amplifier power stage.

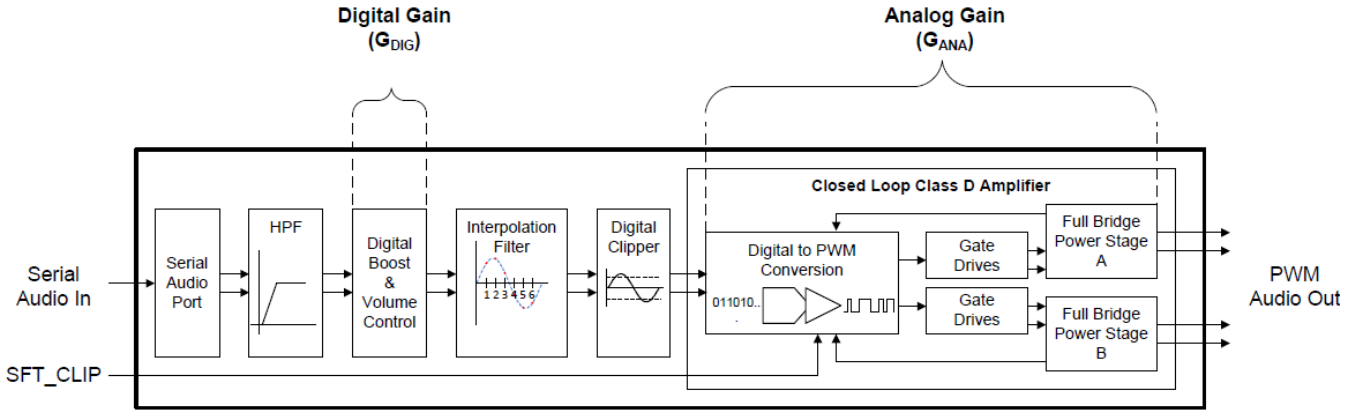


Figure 8 Speaker Amplifier Gain Select

As shown in Figure 8, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to 0dB by default and, in Hardware Control mode, it does not change. For all settings of the GAIN[1:0] pins, the digital boost block remains at +6 dB as analog gain block is transitioned through 19.2, 22.6, and 25 dB.

The values of GDIG and GANA for each of the GAIN[1:0] settings are shown in the table below.

Table. 5 Gain Structure for Hardware Control Mode

GAIN[1:0] pin Setting	Volume Control (dB)	Digital Boost (dB)	Analog Gain (dB)	Total System Gain (dB)
00	0	6	19.2	25.2
01	0	6	22.6	28.6
10	0	6	25	31
11	I²C Control Mode, Gain is controlled via I²C Port			

3.2. I²C Control Mode

In order to place the device in I²C control mode, the two gain pins (GAIN[1:0]) should be pulled HIGH. When this is done, the PBTL/SCL and FREQ/SDA pins are allocated to serve as the clock and data lines for the I²C Control Port.

3.2.1. Speaker Amplifier Shut Down (\SD pin)

In both hardware and I²C Control mode, the \SD pin is provided to place the speaker amplifier into shutdown. The configuration is detailed in section 3.1.1.

3.2.2. Serial Audio Port Controls

In I²C Control mode, additional digital audio data formats and clock rates are made available via the I²C control port. With these controls, the audio format can be set to left justified, right justified, or I²S formatted data.

When used in I²C Control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2 kHz and 96 kHz. The tables below detail the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK Rate the support SCLK rates are shown and are represented in multiples of the sample rate, which is written as "x f_S".

Table. 6 Supported SCLK rates in Double speed mode

Sample Rate fs (kHz)	MCLK rate (× fs)		
	128	192	256
	SCLK rate (× fs)		
88.2	32, 48, 64	32, 48, 64	32, 48, 64
96	32, 48, 64	32, 48, 64	32, 48, 64

3.2.3. Parallel Bridge Tied Load Mode (PBTL)

The HT560 can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the on resistance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of current the speaker amplifier can source before hitting the over-current error threshold.

It should be noted that the device can be placed operated in PBTL mode in either Hardware Control Mode or in I²C Control Mode. For instructions on placing the device in PBTL via the BTL/SCL Pin, see Hardware Control Mode.

To place the HT560 into PBTL Mode when operating in I²C Control Mode, the Bit 3 of Register (0x04) should be set in the control port. This bit is cleared by default to configure the device for BTL mode operation. An additional control available in I²C mode control is PBTL Channel Select, which elects which of the two channels presented on the SDIN line will be used for the input signal for the amplifier. his is found at Bit 7 of (0x16). When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

It is important that before power supplies are brought up, \SD pin should be pulled low. Only after I²C register is programed (including PBTL register), \SD pin can be pulled high.

3.2.4. Speaker Amplifier Gain

As detailed in section 3.1.7, the speaker amplifier gain includes the analog gain and digital gain, both are configured directly in registers when operating in I²C Control mode. It is important to note that the digital boost block is separate from the volume control. The digital boost block should be set before the speaker amplifier is brought out of mute and not changed during normal operation. In most cases, the digital boost can be left in its default configuration, and no further adjustment is necessary.

3.3. I²C Control Port

3.3.1. I²C Device Address

Each device on the I²C bus has a unique address that allows it to appropriately transmit and receive data to and from the I²C master controller. As part of the I²C protocol, the I²C master broadcast an 8-bit word on the bus that contains a 7-bit device address in the upper 7 bits and a read or write bit for the LSB. The HT560 has a configurable I²C address. The SLEEP/ADR can be used to set the device address of the HT560. In I²C Control mode, the seven bit I²C device address is configured as “110110x[R/W]”, where “x” corresponds to the state of the SLEEP/ADR pin at first power up sequence of the device. Upon application of the power supplies, the device latches in the value of the SLEEP/ADR pin for use in determining the I²C address of the device. If the SLEEP/ADR pin is tied LOW at power up (that is connected to the system ground), the device address will be set to 1101100[R/W]. If it is pulled HIGH (that is connected to the DVDD supply), the address will be set to 1101101[R/W] at power up.

[R/W] represents 1 when writing, [R/W] represents 0 when reading.

3.3.2. General Operation of the I²C Control Port

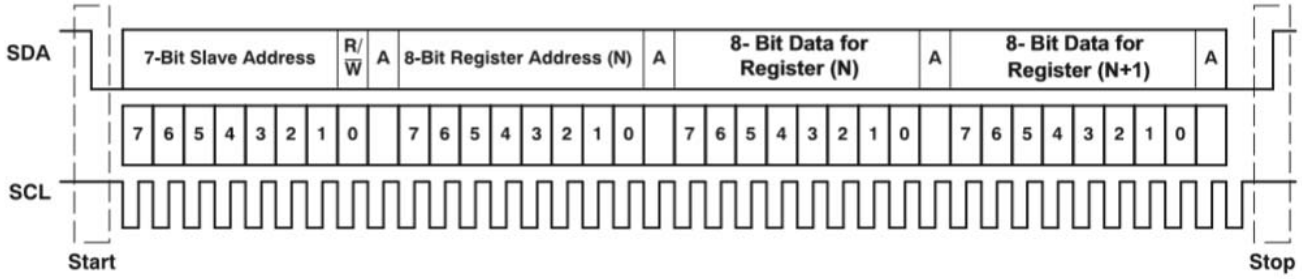


Figure 9 Typical I²C Sequence

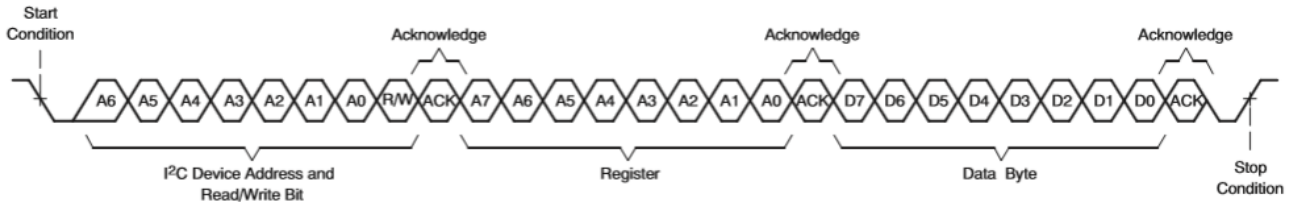


Figure 10 Single-Byte Write Transfer

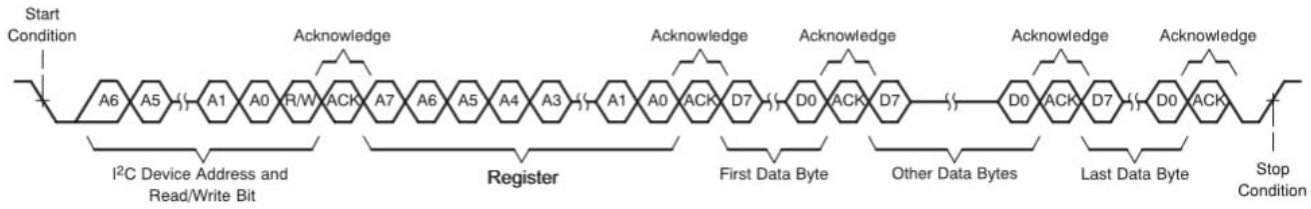


Figure 11 Multiple-Byte Write Transfer

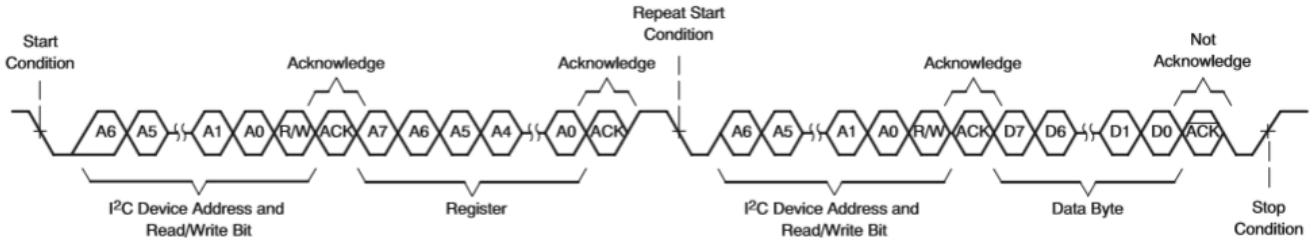


Figure 12 Single-Byte Read Transfer

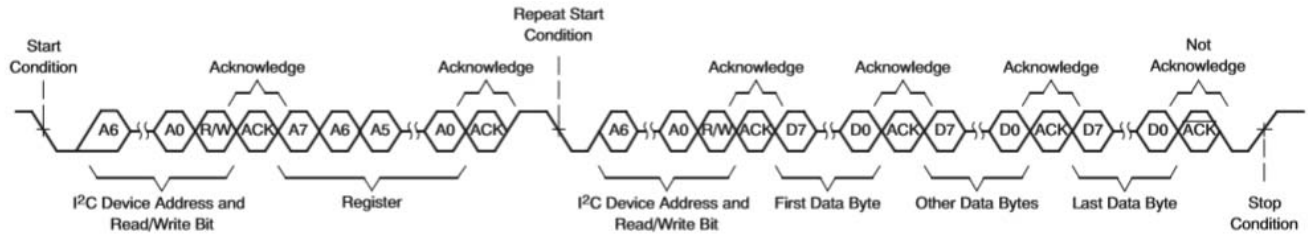


Figure 13 Multiple-Byte Read Transfer

4. *Register Map*

Table. 7 Register Map

Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
0x00	Reserved	Step Pace	LIM	TFB_EN	TFB Attack Time t_{A_TFB}		TFB Release Time t_{R_TFB}		1Ah
0x01	AGC Attack Time t_{A_AGC}				AGC Release Time t_{R_AGC}				97h
0x02	Reserved		Gain						26h
0x03	Modulation	FREQ [1:0]		OCE_{Th}		OTE	OCE	DCE	27h
0x04	Reserved	GAIN [1:0]		FREQ [2]	PBTL	CLKE	Reserved	Reserved	71h
0x05~0x0F	Reserved								
0x10	DigClip[19:12]								FFh
0x11	DigClip[11:4]								FFh
0x12	DigClip[3:0]				SLEEP	SD	MUTE_L	MUTE_R	F4h
0x13	Left channel volume control Vol_L								CFh
0x14	Right channel volume control Vol_R								CFh
0x15	Fade	HPF Byps	Dig Bst	SS/DS	Serial Audio Input Format				94h
0x16	PBTL_ch	Reserved							A0h

The register details are as follows. The blue fonts are the default settings when powering on.

Register Address: 0x00 (default 1Ah)

Bit	R/W	Label	Default	Description	
7	/	Reserved	0	Unused	
6	R/W	Step Pace	0	0: 80 steps,0.25db/step 1: 40 steps,0.5db/step	
5	R/W	LIM	0	Power Limit Mode 0: PCLP function enabled; 1: AGC function enabled	
4	R/W	TFB_EN	1	0: TFB function disabled; 1: TFB function enabled	
3:2	R/W	t_{A_TFB}	10	Thermal Foldback (TFB) Attack Time Setting	
				00: 320ms/step	10: 1280ms/step
				01: 640ms/step	11: 2560ms/step
1:0	R/W	t_{R_TFB}	10	Thermal Foldback (TFB) Release Time Setting	
				00: 640ms/step	10: 2560ms/step
				01: 1280ms/step	11: 5120ms/step

Register Address: 0x01 (default 97h)

Bit	R/W	Label	Default	Description			
7:4	R/W	t_{A_AGC}	1001	AGC Attack Time Setting			
				0000	20μs/step	1000	5.12ms/step
				0001	40μs/step	1001	10ms/step
				0010	80μs/step	1010	20ms/step
				0011	160μs/step	1011	40ms/step
				0100	320μs/step	1100	80ms/step
				0101	640μs/step	1101	Reserved
				0110	1.28ms/step	1110	Reserved
				0111	2.56ms/step	1111	Reserved
3:0	R/W	t_{R_AGC}	0111	AGC Release Time Setting			
				0000	1.28ms/step	1000	1.28ms/step

				0001	2.56ms/step	1001	2.56ms/step
				0010	5.12ms/step	1010	5.12ms/step
				0011	10ms/step	1011	10ms/step
				0100	20ms/step	1100	20ms/step
				0101	40ms/step	1101	Reserved
				0110	80ms/step	1110	Reserved
				0111	160ms/step	1111	Reserved

Note: Do make sure that the release time is longer than attack time.

Register Address: 0x02 (Default 26h)

Bit	R/W	Label	Default	Description
7:6	/	Reserved	00	Unused, make it always 00
5:0	R/W	Gain	26h	Set gain: 00,0000: 6dB 00,0001: 6.5dB ……Gain increased by 0.5dB every step 10,0110: 25dB 10,0111: 25.5dB ……Gain increased by 0.5dB every step 11,1100: 36dB

Register Address: 0x03 (default 27h)

Bit	R/W	Label	Default	Description	
7	R/W	Modulation	0	0: BD mode; 1: 1SPW mode	
6:5	R/W	FREQ[1:0]	01	The amplifier PWM frequency is set by two registers: SPK_CLK [1:0] and SPK_CLK [2]	
4:3	R/W	OCE_{TH}	00	OCE Threshold Setting	
				00:10A	10: 7.5A
				01: 5A	11: 2.5A
2	R/W	OTE	1	Changes to 0 when OTE happened; back to 1 when OTP evacuated;	
1	R/W	OCE	1	Changes to 0 when OCE happened; back to 1 when OCP evacuated;	
0	R/W	DCE	1	Changes to 0 when DCE happened; back to 1 when DCP evacuated;	

Register Address: 0x04 (default 71h)

Bit	R/W	Label	Default	Description	
7	/	Reserved	0	Unused, make it always 0	
6:5	R/W	GAIN [1:0]	11	Analog Gain Setting	
				00: 19.2dB	10: 25dB
				01: 22.6dB	11: depends on 0x02
4	R/W	FREQ [2]	1	The amplifier PWM frequency is set by two registers: FREQ [1:0] and FREQ [2]. Please notice that a PWM frequency between 300kHz and 600kHz will get a better performance for the Class D amplifier. Detailed recommendations for the SPK_CLK selection are listed in Table. 8. The following is the setting for SPK_CLK [2:0]	
				000: FREQ = 6*fs	001: FREQ =8*fs
				010: FREQ =10*fs	011: FREQ =12*fs
				100: FREQ =14*fs	101: FREQ =16*fs
				110: FREQ =20*fs	111: FREQ =24*fs

3	R/W	PBTL	0	0: BTL mode; 1: PBTL mode.
2	R/W	CLKE	0	Changes to 1 when CLKE happened; back to 0 when CLKE evacuated;
1	/	Reserved	0	Unused
0	/	Reserved	1	Unused

Table. 8 Recommendations for the FREQ Selection

fs(kHz)	Recommended FREQ	Recommended Amplifier Switching (PWM) frequency (kHz)
12	24*fs	288
16	24*fs	384
24	16*fs	384
32	12*fs	384
38	10*fs	380
44.1	8*fs	352.8
48	8*fs	384
88.2	6*fs	529.2
96	6*fs	576

Register Address: 0x10 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[19:12]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

Register Address: 0x11 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[11:4]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

Register Address: 0x12 (default F4h)

Bit	R/W	Label	Default	Description
7:4	R/W	DigClip[3:0]	1111	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.
3	R/W	SLEEP	0	0: the device is not in the SLEEP mode; 1: the device is in the SLEEP mode.
2	R/W	SD	1	0: the device is shut down; 1: the device is not shut down;
1	R/W	MUTE_L	0	0: the left channel is not muted 1: the left channel is muted
0	R/W	MUTE_R	0	0: the right channel is not muted 1: the right channel is muted

Register Address: 0x13 (Default CFh)

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_L	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB ……Gain decreased by 0.5dB every step 1100,1111: 0dB ……Gain decreased by 0.5dB every step

				0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

Register Address: 0x14 (Default CFh)

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_R	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB ……Gain decreased by 0.5dB every step 1100,1111: 0dB ……Gain decreased by 0.5dB every step 0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

Register Address: 0x15 (default 94h)

Bit	R/W	Label	Default	Description
7	R/W	Fade	1	0: Volume fading is disabled; 1: Volume fading is enabled
6	R/W	HPF Byps	0	0: The internal high-pass filter in the digital path is not bypassed 1: The internal high-pass filter in the digital path is bypassed
5:4	R/W	Dig Bst	01	Digital Boost setting 00: +0dB is added to the signal in the digital path 01: +6dB is added to the signal in the digital path 10: +12dB is added to the signal in the digital path 11: +18dB is added to the signal in the digital path
3	R/W	SS/DS	0	Single Speed / Double speed mode select 0: Serial Audio Port will accept single speed sample rates (that is 32kHz, 44.1kHz, 48kHz) 1: Serial Audio Port will accept double speed sample rates (that is 88.2kHz, 96kHz)
2:0	R/W	Format	100	Serial Audio Input Format 000: Serial audio input format is 24 bits, right justified 001: Serial audio input format is 20 bits, right justified 010: Serial audio input format is 18 bits, right justified 011: Serial audio input format is 16 bits, right justified 100: Serial audio input format is IIS 101: Serial audio input format is 16-24 bits, left justified Settings above 101 are reserved and must not be used

Register Address: 0x16 (Default A0h)

Bit	R/W	Label	Default	Description
7	R/W	PBTL_ch	1	Channel selection for PBTL mode 0: the audio information from the right channel of the serial audio input stream is used 1: the audio information from the left channel of the serial audio input stream is used
6:0	/	Reserved	20h	Unused, make it always 20h.

5. Typical Applications

5.1. Hardware Control Mode

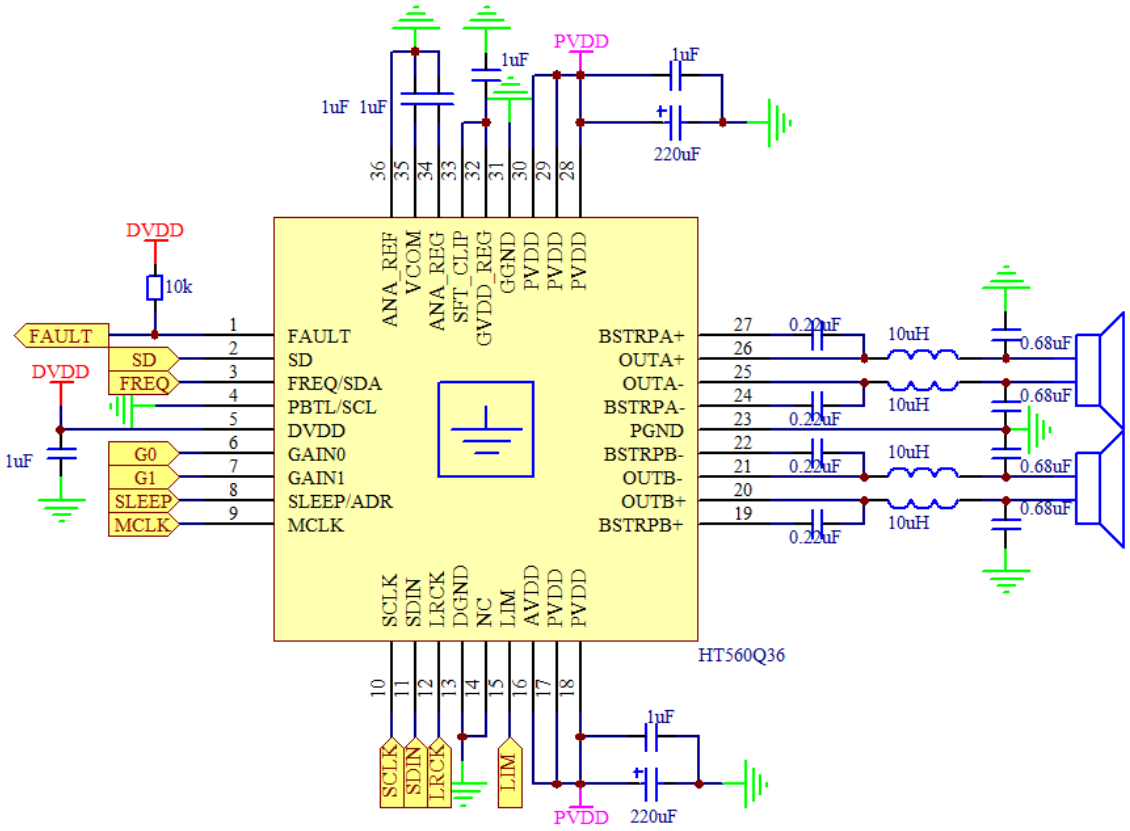
5.1.1. Startup Procedures

1. Configure all hardware pins as required by the application using PCB connections (that is PBTL, FREQ, GAIN, SLEEP, etc.)
2. \SD pin = Low;
3. Bring up power supplies (it does not matter if PVDD, AVDD or DVDD comes up first, provided the device is held in shutdown);
4. Once power supplies are stable, start MCLK, SCLK, LRCK;
5. Once power supplies and clocks are stable and all hardware control pins have been configured, bring \SD pin High;
6. The device is now in normal operation.

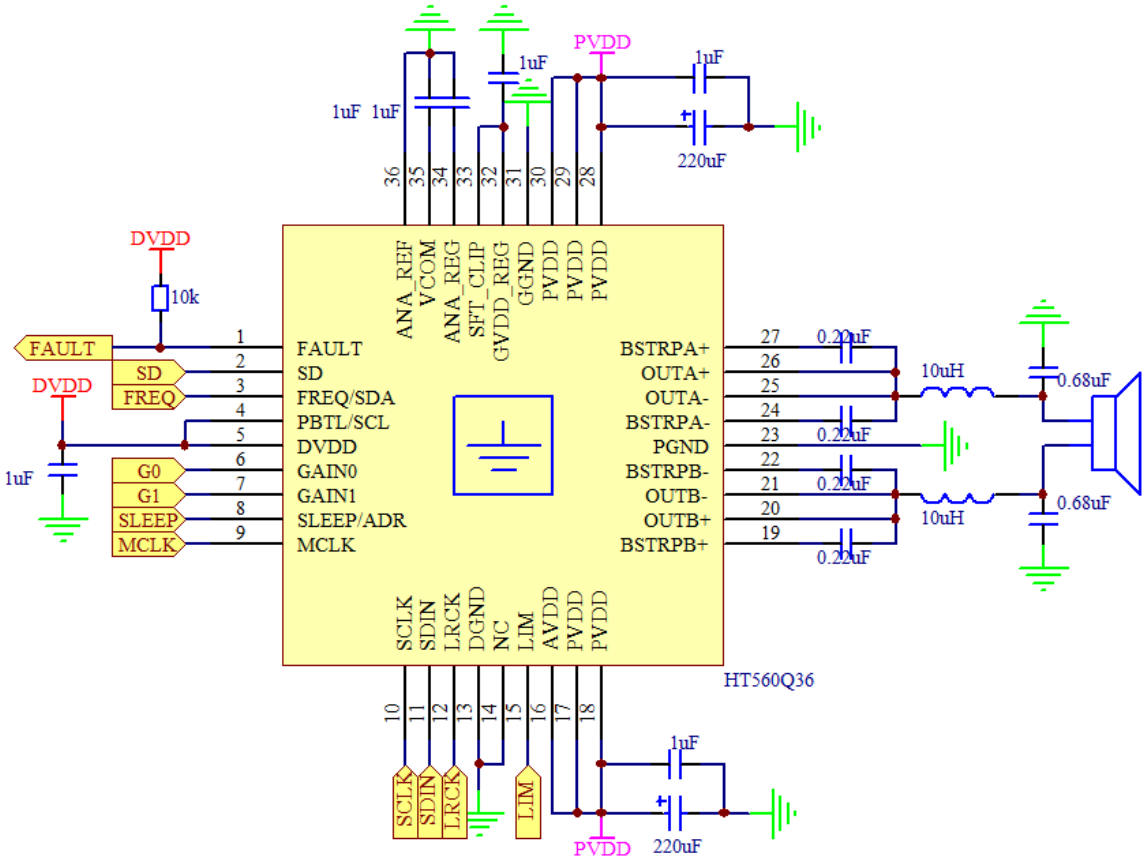
5.1.2. Power down Procedures

1. The device is in normal operation;
2. Pull \SD pin Low;
3. The clocks can be stopped, and power supplies brought down;
4. The device is now fully shutdown and powered off.

5.1.3. Circuit Diagrams



Stereo BTL Using Hardware Control



Mono PBTL Using Hardware Control

5.2. Software Control Mode

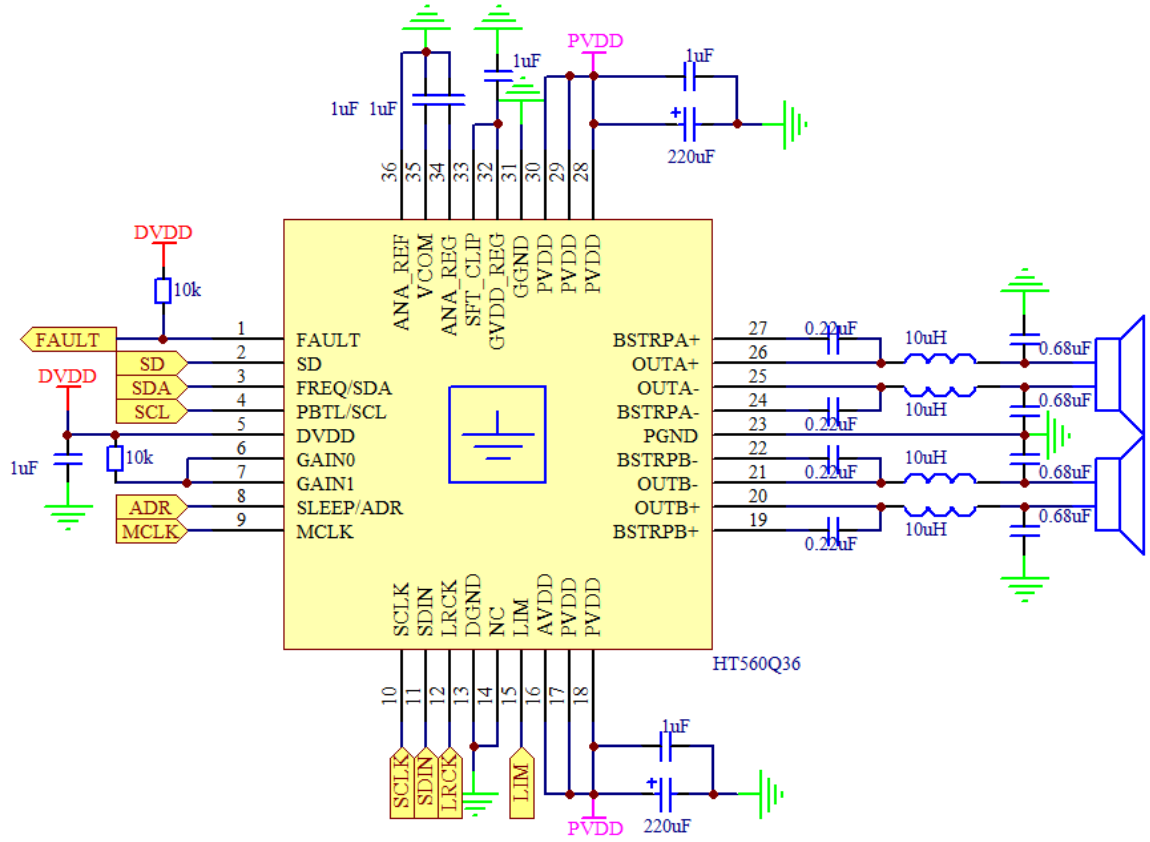
5.2.1. Startup Procedures

1. Configure all digital I/O pins as required by the application using PCB connections (GAIN[1:0] = 11, ADR);
2. \SD pin = Low;
3. Bring up power supplies (it does not matter if PVDD, AVDD or DVDD comes up first, provided the device is held in shutdown);
4. Once power supplies are stable, start MCLK, SCLK, LRCK;
5. Configure the device via the control port in the manner required by the use case, making sure to mute the device; especially bit “PBTL” and “FREQ”. For instance, if fs = 48kHz and BTL mode is needed, write the register 0x04 into 61h; if fs = 48kHz and PBTL mode is needed, write the register 0x04 into 69h;
6. Once power supplies and clocks are stable and the control port has been programmed, bring \SD pin High;
7. Unmute the device via the control port;
8. The device is now in normal operation.

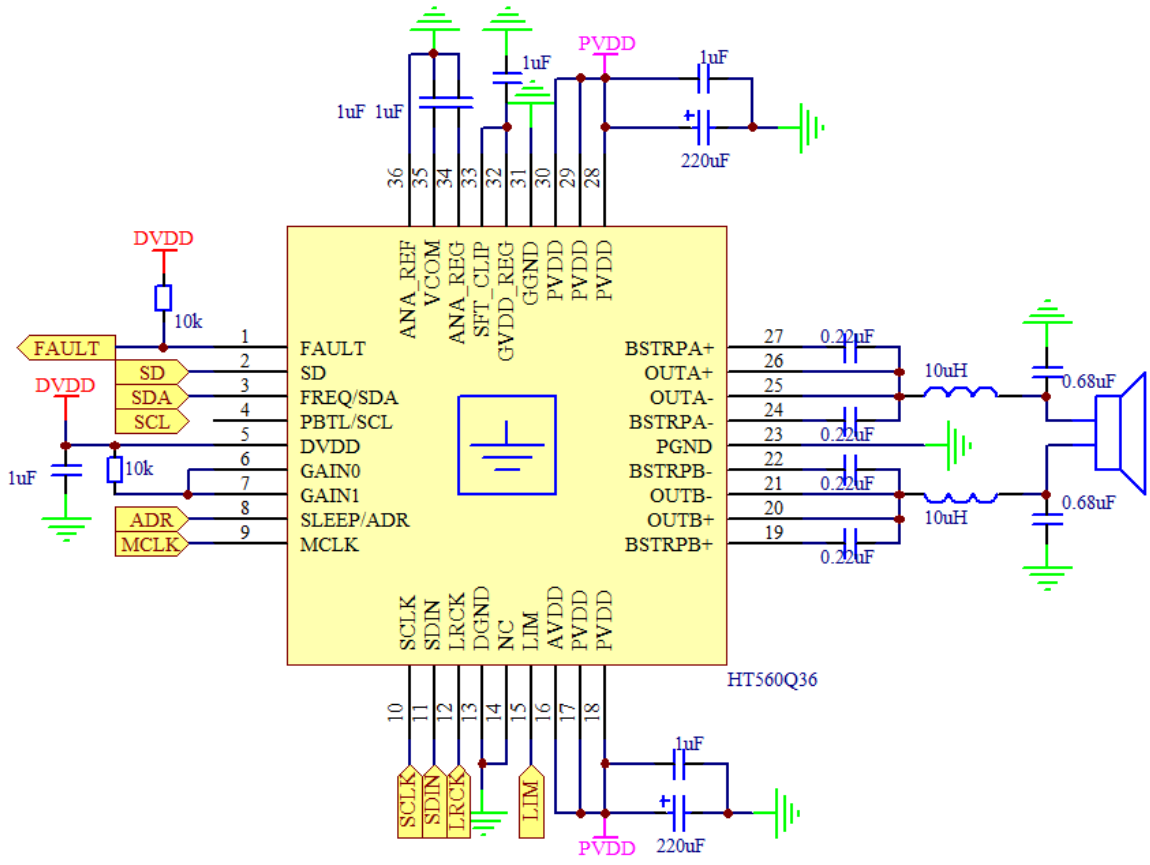
5.2.2. Power down Procedures

1. The device is in normal operation;
2. Mute the device;
3. Pull \SD pin Low;
4. The clocks can be stopped, and power supplies brought down;
5. The device is now fully shutdown and powered off.

5.2.3. Circuit Diagrams



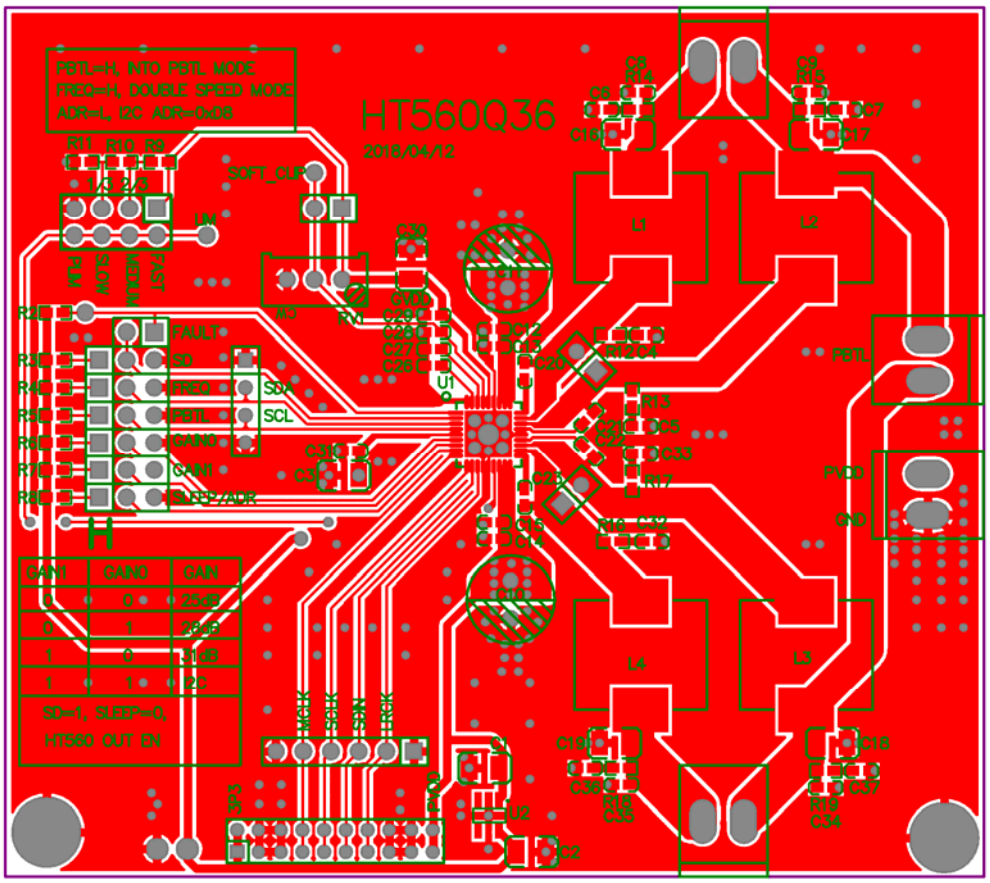
Stereo BTL Using I²C Control



Mono PBTL Using I²C Control

6. PCB Layout

6.1. Top Layout

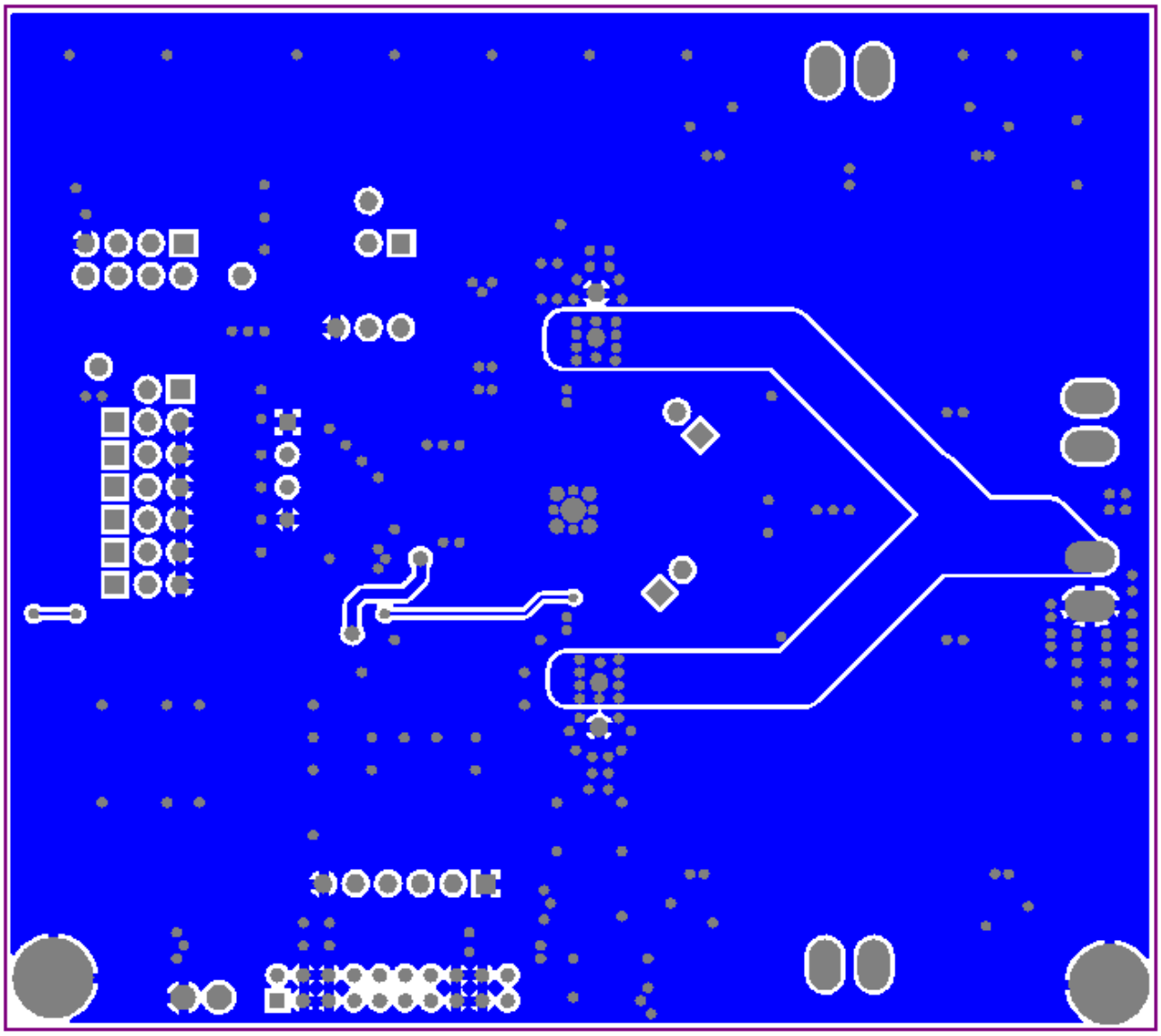


Note1: Connect DGND ang GGND directly to the exposed pad (EP) of the device.

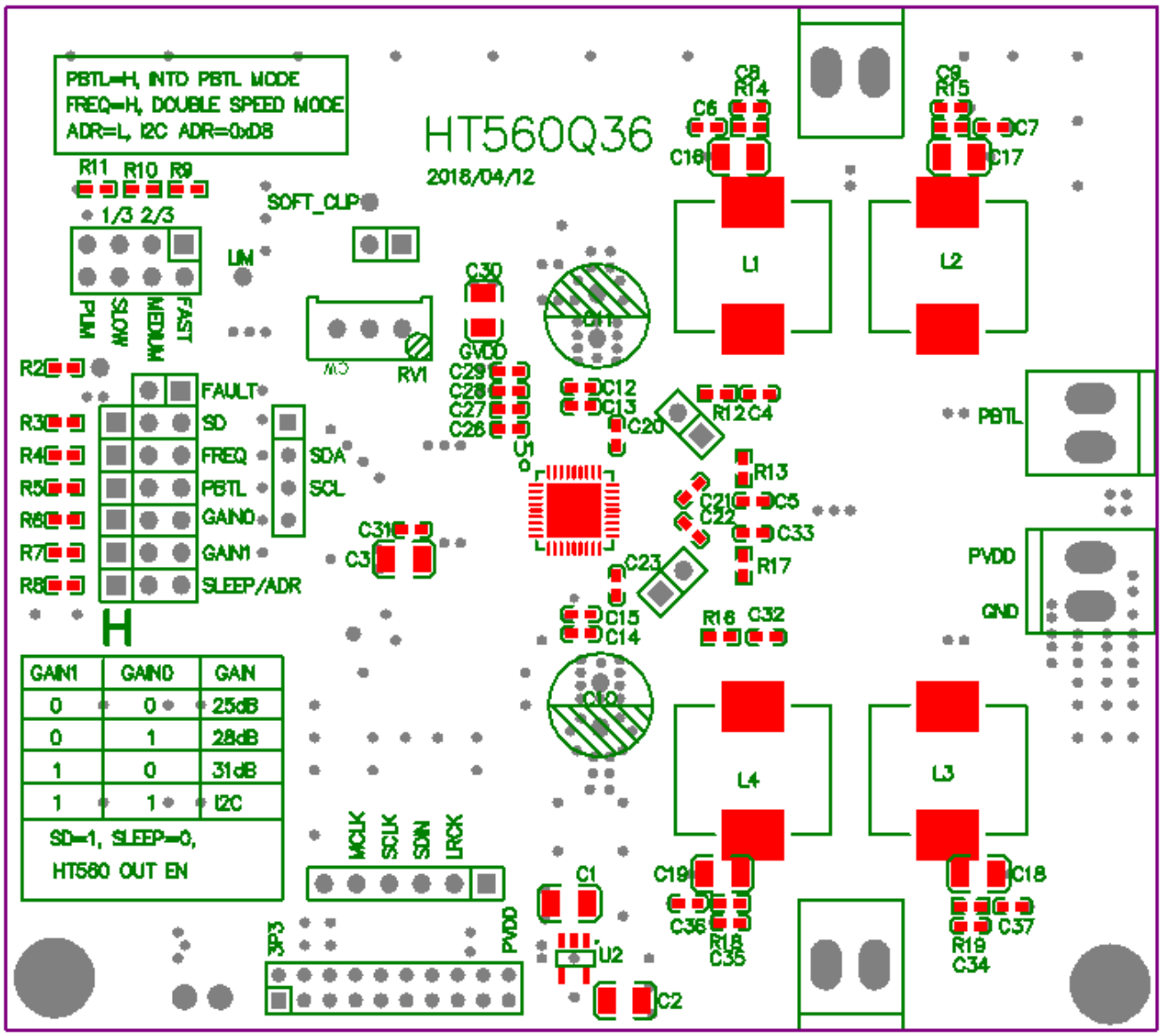
Note2: Connect ANA_REF directly to GND.

Note3: An exposed ground pad must be provided on the PCB, and the exposed pad (EP) of the device should be connected to it via solder closely.

6.2. Bottom Layout

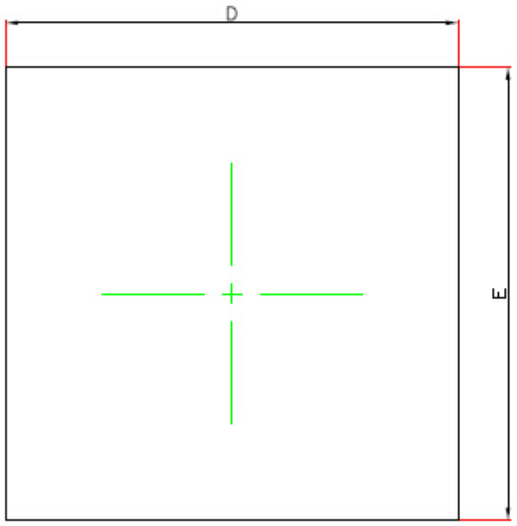


6.3. TopOverlayer

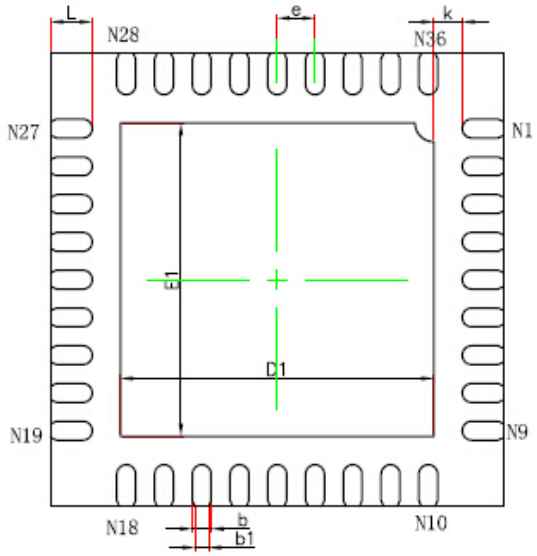


■ PACKAGE OUTLINE

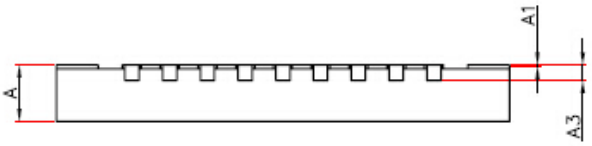
QFN36L 6*6 with exposed thermal pad



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN.	MAX.	MIN.	MAX.
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	5.900	6.100	0.232	0.240
E	5.900	6.100	0.232	0.240
D1	4.050	4.250	0.159	0.167
E1	4.050	4.250	0.159	0.167
b	0.180	0.300	0.007	0.012
b1	0.130	0.230	0.005	0.009
e	0.500TYP.		0.020TYP.	
k	0.200MIN.		0.008MIN.	
L	0.500	0.600	0.020	0.024

IMPORTANT NOTICE
注意

Jiaxing Heroic Electronic Technology Co., Ltd (HT) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any products or services. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

嘉兴禾润电子科技有限公司（以下简称HT）保留对产品、服务、文档的任何修改、更正、提高、改善和其他改变，或停止提供任何产品和服务的权利。客户在下单和生产前应确保所得到的信息是最新、最完整的。

HT assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using HT components.

HT对相关应用的说明和协助以及客户产品的板级设计不承担任何责任。

HT products are not authorized for use in safety-critical applications (such as life support devices or systems) where a failure of the HT product would reasonably be expected to affect the safety or effectiveness of that devices or systems.

HT的产品并未授权用于诸如生命维持设备等安全性极高的应用中。

The information included herein is believed to be accurate and reliable. However, HT assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

本文中的相关信息是精确和可靠的，但HT并不对其负责，也不对任何可能的专利和第三方权利的侵害负责。

Following are URLs and contacts where you can obtain information or supports on any HT products and application solutions:

下面是可以联系到我公司的相关链接和联系方式：

嘉兴禾润电子科技有限公司
Jiaxing Heroic Electronic Technology Co., Ltd.
地址: 浙江省嘉兴市凌公塘路3339号JRC大厦A座三层
Add: A 3rd floor, JRC Building, No. 3339, LingGongTang Road, Jiaxing, Zhejiang Province
Sales: 0573-82585539, sales@heroic.com.cn
Support: 0573-82586151, support@heroic.com.cn
Fax: 0573-82585078
Website: www.heroic.com.cn; wap.heroic.com.cn
Wechat MP: HEROIC_JX
请及时关注禾润官方微信公众号，随时获取最新产品信息和技术资料！