2*75W I²S Input Stereo Class D Amplifier

2×75W I²S Input, Inductor Free, Stereo Class D Amplifier

■ FEATURES

・Power supply: 4.5V – 26.4V
・Audio Performance
- Output Power (BTL)
2×75W (PVDD=24V, RL=4Ω, THD+N=10%)
- Output Power (PBTL)
140W (PVDD=24V, RL=2Ω, THD+N=10%)
- THD+N=0.03% (PVDD=24V, RL=4Ω, Po=1W)
- Noise: 75uV (Gain = 25.2dBV, A weighted)
・Audio I/O Configuration
- Single Stereo I²S Input
- BTL or PBTL output
- 32, 44.1, 48, 88.2, 96kHz Sample Rates
・General Operational Features
- Selectable Hardware or I²C Control mode
- Integrated Digital Output Clipper and AGC
- Integrated Thermal Foldback Function
- Programmable I²C Address (110110x[R/W])
- Adjustable Switching Frequency for Class D
・Robustness Features
- Clock Error, DC, and Short-Circuit Protection
- Overtemperature and Programmable
- Overcurrent Protection
・Packages: Pb-free Packages, ETSSOP32 (EPAD up)

・电源供电
-PVDD: 4.5V – 26.4V;
・音频性能
- 输出功率(BTL)
2×75W (PVDD=24V, RL=4Ω, THD+N=10%)
- 输出功率(PBTL)
140W (PVDD=24V, RL=2Ω, THD+N=10%)
- THD+N=0.03% (PVDD=24V, RL=4Ω, Po=1W)
-噪声: 75uV (Gain = 25.2dBV, A加权)
・音频I/O:
- I²S输入
- BTL或PBTL输出
- 32, 44.1, 48, 88.2, 96kHz采样频率
・其他功能
- 硬件模式或I²C控制模式
- 数字限幅器和AGC功能
- 限温控制
- I²C地址可选(110110x[R/W])
- D类PWM频率可调
・保护：时钟错误、直流、短路保护等；过温保护，可设置；过流保护
・ETSSOP32封装(顶部散热片)

■ APPLICATIONS

・Bluetooth/Wi-Fi Speakers ・Portable Speakers
・Smart speakers ・LCD TV/Monitor
・Sound Bars, Docking stations, PC Audio

・蓝牙/ Wi-Fi音箱 ・便携式音箱
・智能音箱 ・LCD TV/监视器
・声霸, 扩展坞, PC音频 ・

■ DESCRIPTION

The HT5606 is a stereo Class D audio amplifier with an I²S input serial port. It supports a variety of audio clock configurations via two speed modes.

The outputs of the HT5606 can be configured to drive two speakers in stereo BTL mode or mono PBTL mode.

The HT5606 also includes hardware and I²C control modes, integrated digital clipper, AGC, several gain options, and a wide power supply operating range to enable use in a multitude of applications.

An optimal mix of thermal performance and device cost is provided in the 110-mΩ RDS(ON) of the output MOSFETs. Additionally, a thermally enhanced ETSSOP32 (EPAD up) provides excellent operation in the elevated ambient temperatures found in modern consumer electronic devices.

HT5606是一颗I²S输入的立体声D类音频功放，支持多种采样频率，包含两种速率模式。

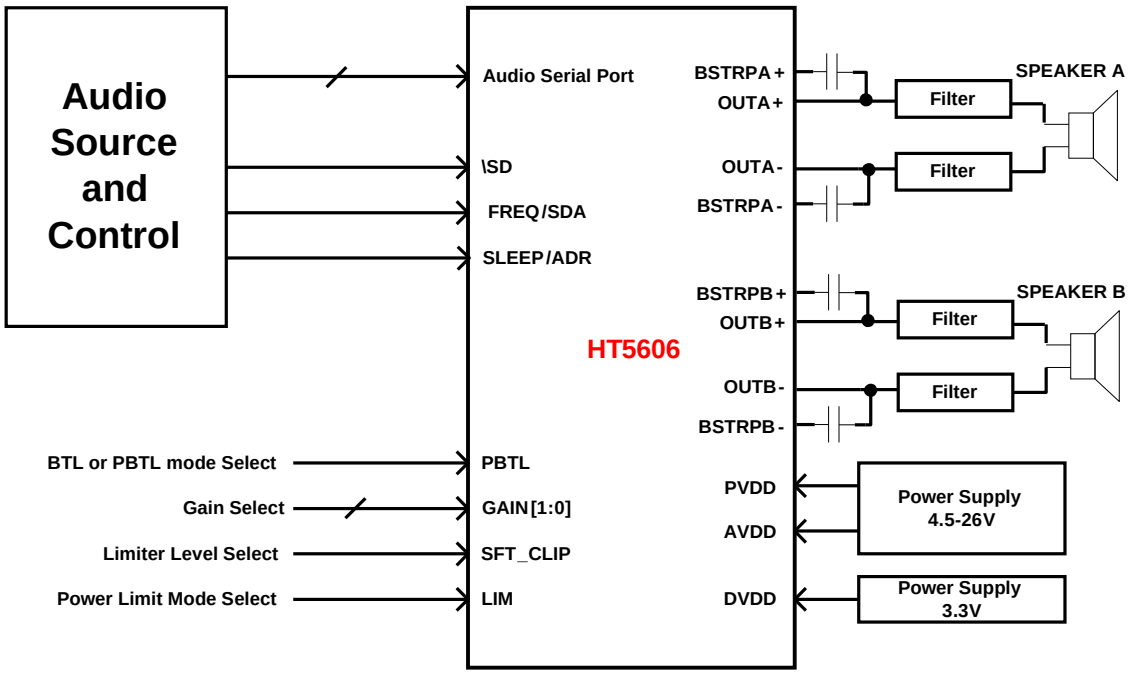
HT5606除了驱动BTL立体声双喇叭外，还能驱动PBTL单喇叭。

HT5606包含了硬件工作模式和I²C控制模式，具有数字限幅器、AGC、多种增益选择，支持不同应用下较宽的工作电压范围。

功放输出MOS的$R_{DS(ON)}$约为110mΩ，其在成本和散热二者间达到了最佳平衡。

该产品提供ETSSOP32封装（顶部散热片），其具有不错的散热表现，在现代消费电子复杂的环境温度下提供出色的性能。

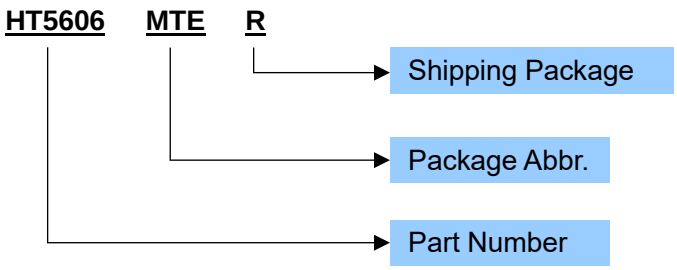
■ TYPICAL APPLICATION



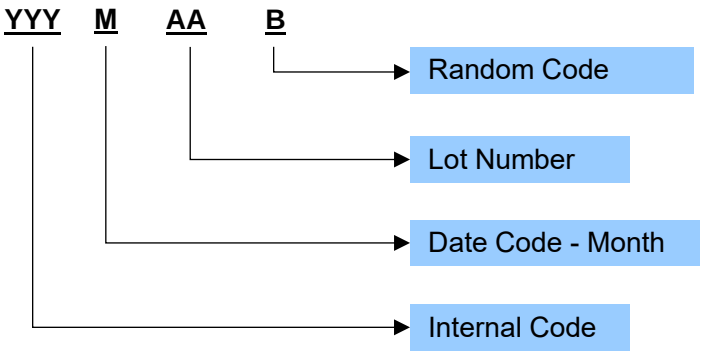
■ ORDERING INFORMATION

Part Number	Package Type	Package Abbr.	Eco Plan	MSL Level	Marking	Shipping Package / MOQ
HT5606MTER	ETSSOP32 (EPAD up)	MTE	RoHS	MSL3	HT5606 YYYMAAB[1]	Tape and Reel (R) / 2000pcs

Part Number

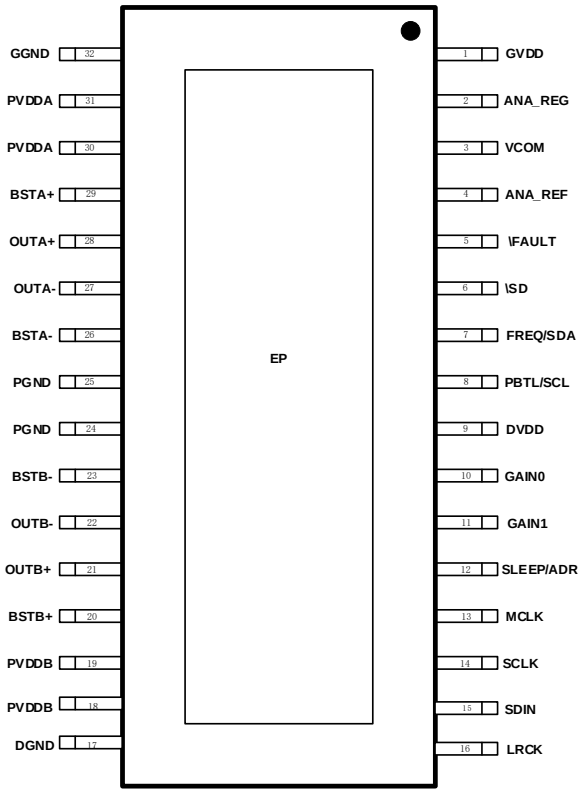


Production Tracking Code



[1] YYYMAAB is production tracking code

■ TERMINAL CONFIGURATION



Top View

■ TERMINAL FUNCTION

Terminal No.	Name	I/O[1]	Description
32	GGND	G	Ground for gate drive circuitry (this terminal should be connected to the system ground). 栅极驱动电路地
31,30	PVDDA	P	Power Supply for internal power circuitry of Channel A. A声道功率电源
29	BSTA+	BST	Connection point for the OUTA+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTA. OUTA+自举电容位
28	OUTA+	O	Positive pin for differential speaker amplifier output A. A声道输出正端
27	OUTA-	O	Negative pin for differential speaker amplifier output A. A声道输出负端
26	BSTA-	BST	Connection point for the OUTA- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTA-. OUTA-自举电容位
25,24	PGND	G	Ground for power device circuitry (NOTE: This terminal should be connected to the system ground). 功率地
23	BSB-	BST	Connection point for the OUTB- bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTB-. OUTB-自举电容位
22	OUTB-	O	Negative pin for differential speaker amplifier output B. B声道输出负端
21	OUTB+	O	Positive pin for differential speaker amplifier output B. B声道输出正端
20	BSTB+	BST	Connection point for the OUTB+ bootstrap capacitor, which is used to create a power supply for the high-side gate drive for OUTB+. OUTB+自举电容位
19,18	PVDDB	P	Power Supply for internal power circuitry of Channel B. B声道功率电源
17	DGND	G	Ground for digital circuitry (NOTE: This pin should be connected to the system ground). 数字地
16	LRCK	I	Word select clock for the digital signal that is active on the serial port's input data line. 帧时钟，字段（声道）选择
15	SDIN	I	Data line to the serial data port. 串行数据
14	SCLK	I	Bit clock for the digital signal that is active on the serial data port's input data line. 串行

[1] I: Input; O: Output; G: Ground; P: Power; BST: BOOT Strap; OD: Open drain

			时钟
13	MCLK	I	Master Clock used for internal clock tree, sub-circuit/state machine, and Serial Audio Port clocking. 主时钟
12	SLLEP/ADR	I	In Hardware Control Mode, places the speaker amplifier in sleep mode. In I²C Control Mode, is used to determine the I²C Address of the device I²C控制模式时为I²C器件地址选择pin；硬件模式时，为SLEEP模式设置引脚
11	GAIN1	I	Adjusts the MSB of the multi-bit gain of the speaker amplifier. 增益设置脚高位
10	GAIN0	I	Adjusts the LSB of the multi-bit gain of the speaker amplifier. 增益设置脚低位
9	DVDD	P	Power supply for the internal digital circuitry. 数字电源端
8	PBTL/SCL	I	Dual function pin that functions as an I²C clock input terminal in I²C Control Mode or configures the device to operate in pre-filter Parallel Bridge Tied Load (PBTL) mode when in Hardware Control Mode. I²C控制模式时为I²C时钟pin；硬件模式时，为PBTL模式设置引脚
7	FREQ/SDA	I	Dual function pin that functions as an I²C data input pin in I²C Control Mode or as a Frequency Select terminal when in Hardware Control Mode. I²C控制模式时为I²C数据pin；硬件模式时，为频率设置引脚
6	\SD	I	Places the speaker amplifier in shutdown mode while pulled low level. 接地时功放关闭
5	\FAULT	OD	Speaker amplifier fault terminal, which is pulled LOW when an internal fault occurs, open-drain output. 错误状态位，芯片发生某些错误时，该引脚拉低
4	ANA_REF	P	Connection point for internal reference used by ANA_REG and VCOM filter capacitors. And connect to system GND net. ANA_REG 和 VCOM的滤波电容的参考点，接地
3	VCOM	P	Bias voltage for internal PWM conversion block. 内部PWM转换模块的偏置电压
2	ANA_REG	P	Voltage regulator derived from AVDD supply (NOTE: This terminal is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry). 内部整流输出，接1uF电容到地
1	GVDD	O	Voltage regulator derived from PVDD supply (NOTE: This pin is provided as a connection point for filtering capacitors for this supply and must not be used to power any external circuitry). 内部整流输出，接1uF电容到地
/	EP	-	Thermal pad up, must be good connected to heat-sink for power dissipation. 顶部散热片，需连接至外部散热器

■ SPECIFICATIONS[1]

● Absolute Maximum Ratings [2]

PARAMETER	Symbol	MIN	TYP	MAX	UNIT
Power supply voltage for AVDD	AVDD	-0.3		30	V
Power supply voltage for PVDD	PVDD	-0.3		30	V
Power supply voltage for DVDD	DVDD	-0.3		4	V
DVDD Referenced Digital Input Voltages	V_I	−0.3		DVDD+0.3	V
Analog Input Voltage (SFT_CLIP, LIM)	V_I	−0.3		GVDD	V
Moisture Sensitivity Level (MSL)			MSL3		
Ambient Operating Temperature	T_A	-25		85	℃
Storage Temperature	T_{STG}	-40		125	℃

● Recommended Operating Conditions

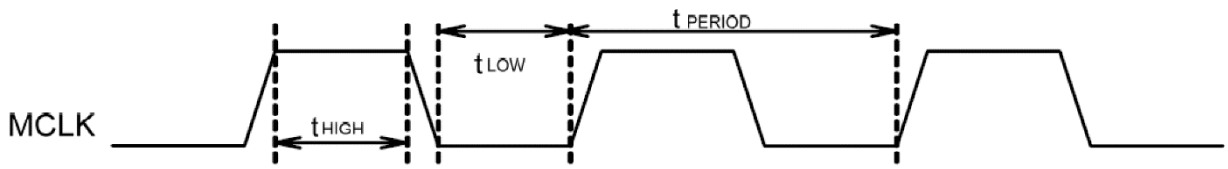
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Power supply voltage for AVDD	AVDD		4.5		26.4	V
Power supply voltage for PVDD	PVDD		4.5		26.4	V
Power supply voltage for DVDD	DVDD		2.8	3.3	3.63	V
Ambient Operating Temperature	T_a		-25	25	85	℃
Junction Temperature	T_J		-40		125	℃
DVDD Referenced Digital Input Voltages	V_I		0		DVDD	V
Analog Input Voltage (SFT_CLIP, LIM)	V_I		0		GVDD	V
Minimum Speaker Load in BTL Mode	R_L		4			Ω
Minimum Speaker Load in PBTL Mode	R_L		2			Ω

● I/O pins

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Input Logic High threshold for DVDD referenced digital inputs	V_{IH1}	All Digital I/O pins including \FAULT, \SD, FREQ/SDA, PBTL/SCL. PBTL/SCL, GAIN0, GAIN1, SLLEP/ADR, MCLK, SCLK, SDIN, LRCK	70			%DVDD
Input Logic LOW threshold for DVDD Referenced Digital Inputs	V_{IL1}				30	%DVDD
Input Logic HIGH Current Level	I_{IH1}				15	uA
Input Logic LOW Current Level	I_{IL1}				-15	uA
Output Logic LOW Voltage Level	V_{OH}		90			%DVDD
Output Logic LOW Voltage Level	V_{OL}				10	%DVDD
Analog Input Voltage	V_I	SFT_CLIP, LIM	0		GVDD	V

● Master Clock

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable MCLK Duty Cycle	D_{MCLK}		45	50	55	%
Supported MCLK Frequencies	f_{MCLK}	Values include: 128, 192, 256, 384, 512.	128		512	f_s
Pulse duration of MCLK high	t_{HIGH}		20.2			ns
Pulse duration of MCLK low	t_{LOW}		20.2			ns
Period of MCLK	t_{PERIOD}		40.4			ns

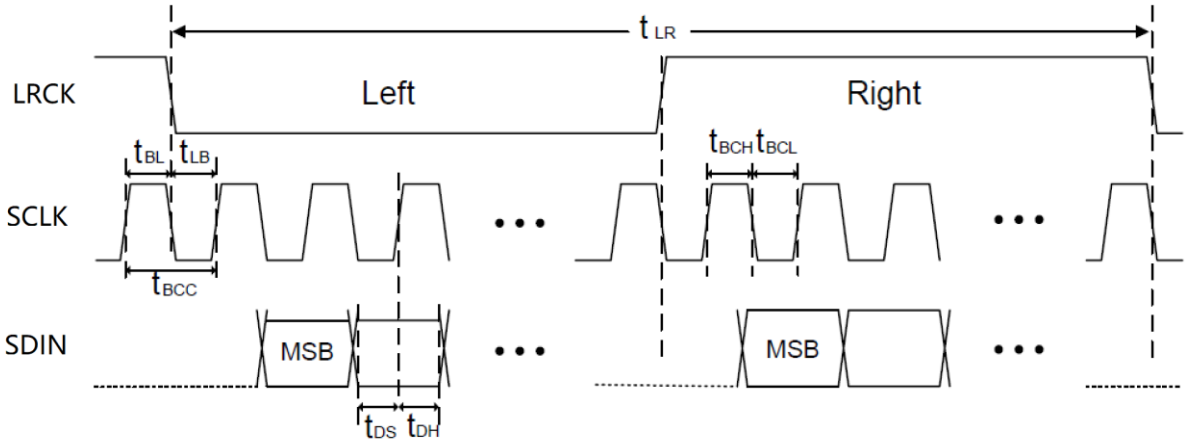


[1] Depending on parts and PCB layout, characteristics may be changed.

[2] Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

Serial Audio Port

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Allowable SCLK Duty Cycle	D_{SCLK}		45	50	55	%
Supported Input Sample Rates ($1/t_{LR}$)	f_s		32		96	kHz
Required LRCK to SCLK Rising Edge	t_{LB}		15			ns
Required SCLK Rising Edge to LRCK edge	t_{BL}		15			ns
Supported SCLK Frequencies ($1/t_{BCC}$)	F_{SCLK}	Values include: 32, 48, 64	32		64	f_s
SCLK Pulse Width High	t_{BCL}			$t_{BCC}/2$		
SCLK Pulse Width Low	t_{BCH}			$t_{BCC}/2$		
Required SDIN Hold Time after SCLK, Rising Edge	t_{DH}		15			ns
Required SDIN Setup Time before SCLK Rising Edge	t_{DS}		15			ns



Protection Circuitry

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
PVDD Overvoltage Error Threshold	OVE_{RTH}	PVDD Rising		28		V
PVDD Overvoltage Error Threshold	OVE_{FTH}	PVDD Falling		27		V
PVDD Undervoltage Error Threshold	UVE_{RTH}	PVDD Falling		4.2		V
PVDD Undervoltage Error Threshold	UVE_{FTH}	PVDD Rising		4.4		V
Overtemperature Error Threshold	OTE_{TH}			150		℃
Overtemperature Error Hysteresis	OTE_{HYS}			15		℃
Thermal foldback trig point	TFB			135		℃
Thermal Foldback Attack Time	t_{A_TFB}			1200		ms/dB
Thermal Foldback Release Time	t_{A_TFB}			2400		ms/dB
Overcurrent Error Threshold for each BTL Output	OCE_{TH}	OCE_{TH} = 00		10		A
DC Error Threshold	DCE_{TH}			2.6		V
Speaker Amplifier Fault Time Out period	T_{fault}	DCE		650		ms
		DCE or OCP		1.3		s

- **Speaker Amplifier in All Modes**

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 00	AV_{00}			25.2		dBV
Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 01	AV_{01}			28.6		dBV
Speaker Amplifier Gain with SPK_GAIN[1:0] Pins = 10	AV_{10}			31		dBV
Speaker Amplifier Gain with SPK_GAIN[1:0] Pins =11	AV_{11}		(Set via I²C)			
Speaker Amplifier DC Offset	$\lvert V_{OS} \rvert$	BTL		5		mV
		PBTL		10		mV
Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 1	$f_{SPK\_AMP(1)}$			16		f_S
Speaker Amplifier Switching Frequency when PWM_FREQ Pin = 0	$f_{SPK\_AMP(0)}$			8		f_S
On Resistance of Output MOSFET (both high-side and low-side)	$R_{DS(ON)}$			120		mΩ
–3-dB Corner Frequency of High-Pass Filter	f_C	f_S = 44.1 kHz		3.7		Hz
		f_S = 48 kHz		4		Hz
		f_S = 88.2 kHz		7.4		Hz
		f_S = 96 kHz		8		Hz

- **Speaker Amplifier in Stereo Bridge Tied Load (BTL) Mode**

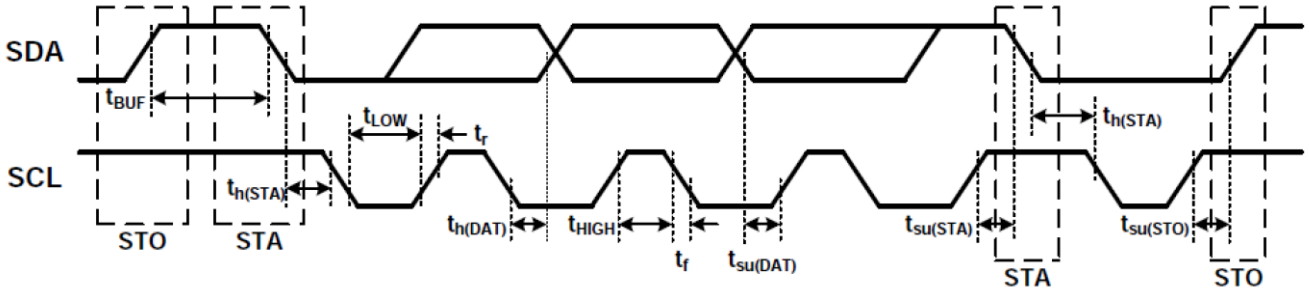
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V_N	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω or 4 Ω, 20-20kHz, A-Weighted		74		μVrms
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8 Ω or 4Ω, 20-20kHz, A-Weighted		140		μVrms
Signal to Noise Ratio (Referenced to THD+N=1%)	SNR	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω or 4Ω, 20-20kHz, A-Weighted		98		dB
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8 Ω or 4Ω, 20-20kHz, A-Weighted		100		dB
Maximum Output Power Per. Ch.	Po	PVDD = 12 V, R_{SPK} = 4 Ω, THD+N = 1%		15		W
		PVDD = 12 V, R_{SPK} = 8 Ω, THD+N = 1%		8.4		W
		PVDD = 15 V, R_{SPK} = 4 Ω, THD+N = 1%		22.5		W
		PVDD = 15 V, R_{SPK} = 8 Ω, THD+N = 1%		13		W
		PVDD = 18 V, R_{SPK} = 4 Ω, THD+N = 1%		25		W
		PVDD = 18 V, R_{SPK} =8 Ω, THD+N = 1%		18.5		W
		PVDD = 24 V, R_{SPK} = 4 Ω, THD+N = 1%		60		W
		PVDD = 24 V, R_{SPK} = 8 Ω, THD+N = 1%		32		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R_{SPK} = 4 Ω, Po = 1 W		0.05		%
		PVDD = 12 V, R_{SPK} =8 Ω, Po = 1 W		0.03		%
		PVDD = 15 V, R_{SPK} = 4 Ω, Po = 1 W		0.05		%
		PVDD = 15 V, R_{SPK} = 8 Ω, Po = 1 W		0.025		%
		PVDD = 18 V, R_{SPK} = 4 Ω, Po = 1 W		0.045		%
		PVDD = 18 V, R_{SPK} = 8 Ω, Po = 1 W		0.02		%
		PVDD = 24 V, R_{SPK} = 4 Ω, Po = 1 W		0.04		%
		PVDD = 24 V, R_{SPK} = 8 Ω, Po = 1 W		0.02		%
Cross-talk (worst case between LtoR and RtoL coupling)	X-Talk	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1kHz Sine		-92		dB
		PVDD = 24 V, SPK_GAIN[1:0] Pins = 10, R_{SPK} = 8 Ω, Input Signal 250 mVrms, 1kHz Sine		-93		dB

- **Speaker Amplifier in Mono Parallel Bridge Tied Load (PBTL) Mode**

PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
Idle Channel Noise	V_N	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, A-Weighted		75		μVrms
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8 Ω, A-Weighted		140		μVrms
Signal to Noise Ratio (Referenced to THD+N =1%)	SNR	PVDD = 12 V, SPK_GAIN[1:0] Pins = 00, R_{SPK} = 8 Ω, A-Weighted		99		dB
		PVDD = 24 V, SPK_GAIN[1:0] Pins =10, R_{SPK} = 8 Ω, A-Weighted		100		dB
Maximum Output Power.	Po	PVDD = 12 V, R_{SPK} = 4 Ω, THD+N = 1%		16.5		W
		PVDD = 12 V, R_{SPK} = 8 Ω, THD+N = 1%		8.8		W
		PVDD = 15 V, R_{SPK} = 4 Ω, THD+N = 1%		25.7		W
		PVDD = 15 V, R_{SPK} = 8 Ω, THD+N = 1%		13.8		W
		PVDD = 18 V, R_{SPK} = 4 Ω, THD+N = 1%		36.9		W
		PVDD = 18 V, R_{SPK} = 8 Ω, THD+N = 1%		19.7		W
		PVDD = 24 V, R_{SPK} = 2 Ω, THD+N = 1%		113.5		W
		PVDD = 24 V, R_{SPK} = 4 Ω, THD+N = 1%		64		W
		PVDD = 24 V, R_{SPK} = 8 Ω, THD+N = 1%		34.8		W
Total Harmonic Distortion and Noise	THD+N	PVDD = 12 V, R_{SPK} = 4 Ω, Po = 1 W		0.036		%
		PVDD = 12 V, R_{SPK} = 8 Ω, Po = 1 W		0.018		%
		PVDD = 15 V, R_{SPK} = 4 Ω, Po = 1 W		0.035		%
		PVDD = 15 V, R_{SPK} = 8 Ω, Po = 1 W		0.017		%
		PVDD = 18 V, R_{SPK} = 4 Ω, Po = 1 W		0.035		%
		PVDD = 18 V, R_{SPK} = 8 Ω, Po = 1 W		0.017		%
		PVDD = 24 V, R_{SPK} = 4 Ω, Po = 1 W		0.034		%
		PVDD = 24 V, R_{SPK} = 8 Ω, Po = 1 W		0.017		%

- **I²C Control Port**

PARAMETER	Symbol	Standard-Mode			Fast-Mode			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Allowable Load Capacitance for Each I²C Line	C_b			400			400	pF
Support SCL frequency	f_{SCL}			100			400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{h(STA)}$	4			0.6			us
Required Pulse Duration, SCL HIGH	t_{HIGH}	4			0.6			us
Required Pulse Duration, SCL LOW	t_{LOW}	4.7			1.3			us
Setup time for a repeated START condition	$t_{su(STA)}$	4.7			0.6			us
Data hold time	$t_{h(DAT)}$	0		3.45	0		0.9	us
Setup Time, SDA to SCL	$t_{su(DAT)}$	250			100			ns
Rise Time, SCL	T_{r_SCL}			1000			300	ns
Rise Time, SDA	T_{r_SDA}			$1/(4*f_{scl})$-0.25			$1/(4*f_{scl})$-0.25	us
Fall Time, SCL and SDA	T_f			300			300	ns
Setup Time, SCL to STOP condition	$t_{su(STO)}$	4			0.6			us
Bus Free time between STOP and START conditions	t_{BUF}	4.7			1.3			us



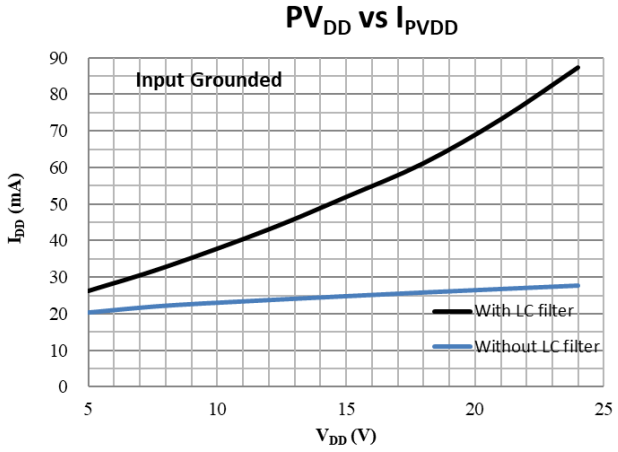
Typical current consumption

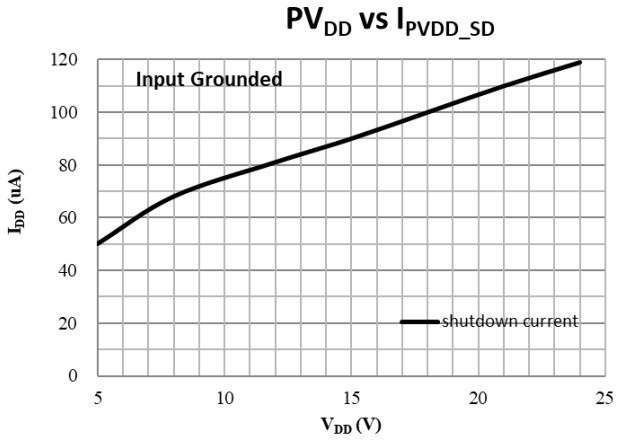
TA = 25°, PVDD = 12V, DVDD= 3.3V, No Load, BTL mode, fs = 48kHz, fspk_amp=384kHz(unless otherwise noted)

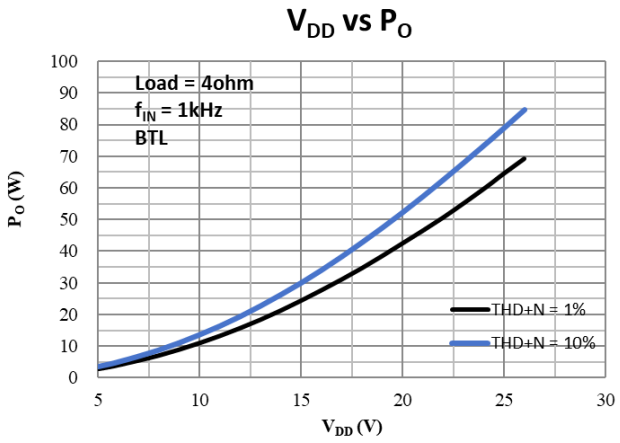
PARAMETER	Symbol	CONDITION	MIN	TYP	MAX	UNIT
IDVDD						
Quiescent current in DVDD	I_{DVDD}	fs=48kHz MCLK=128*fs		2.91		mA
		fs=48kHz MCLK=256*fs		3.89		mA
		fs=48kHz MCLK=512*fs		4.67		mA
		fs=32kHz MCLK=128*fs		2.24		mA
		fs=32kHz MCLK=256*fs		2.89		mA
		fs=32kHz MCLK=512*fs		3.44		mA
DVDD current consumption in sleep mode	I_{DVDD_SLEEP}	SLEEP = H, fs=48kHz MCLK=256*fs		2.15		mA
		SLEEP = H, fs=32kHz MCLK=256*fs		1.97		mA
DVDD current consumption in SD mode	I_{DVDD_SD}	\SD = L, No clock		45		uA
IPVDD						
Quiescent current in PVDD	IPVDD	PVDD=12V fs=48kHz MCLK=256*fs		23.9		mA
		PVDD=24V fs=48kHz MCLK=256*fs		27.9		mA
		PVDD=12V fs=32kHz MCLK=256*fs		20.5		mA
		PVDD=24V fs=32kHz MCLK=256*fs		23.3		mA
PVDD current consumption in sleep mode	I_{PVDD_SLEEP}			14		mA
PVDD current consumption in SD mode	I_{PVDD_SD}	PVDD=12V		100		uA
		PVDD=24V		150		uA

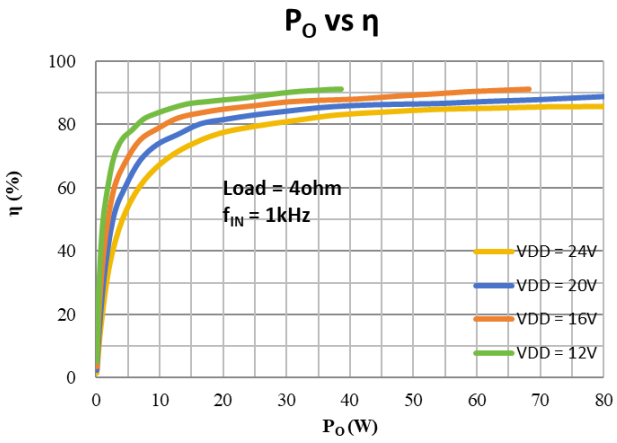
■ TYPICAL OPERATING CHARACTERISTICS

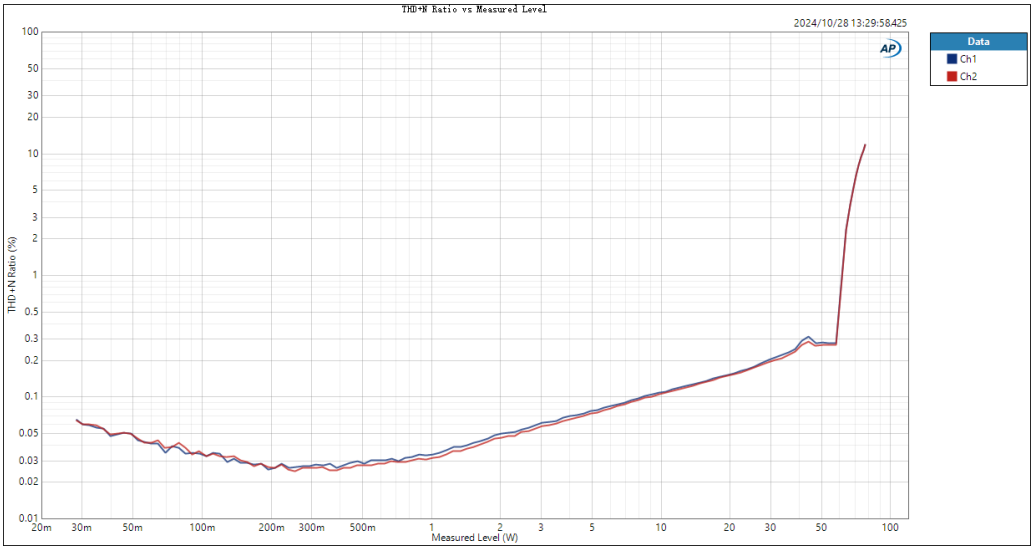
T_A = 25°C, **BTL mode**, f_{SPK_AMP} = 384 kHz, f_{IN} = 1 kHz, unless otherwise noted. Output filter is used as 15 μH and 0.68 μF, unless otherwise noted.



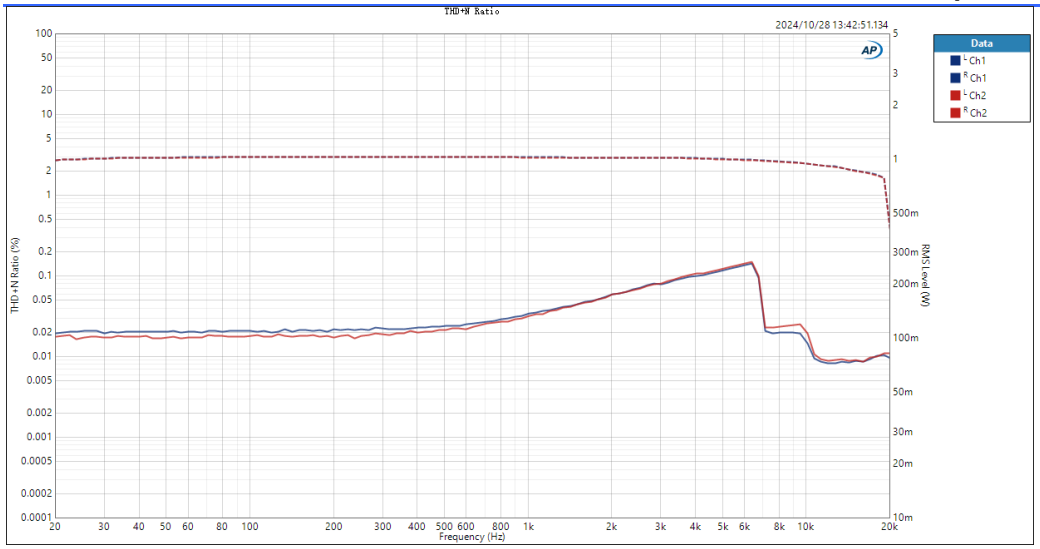








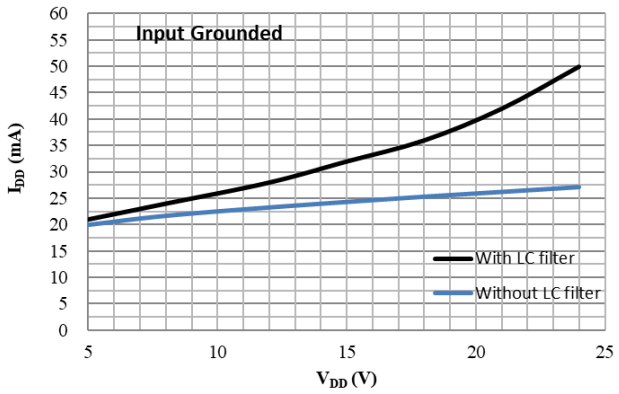
THD+N vs Po, 24V, 4ohm



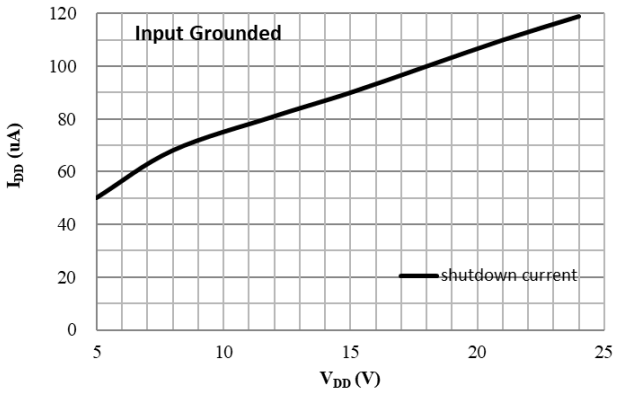
THD+N vs f_{IN}, 24V, 4ohm

T_A = 25°C, **PBTL mode**, f_{SPK_AMP} = 384 kHz, f_{IN} = 1 kHz, unless otherwise noted. Output filter is used as 10 μH and 0.68 μF, unless otherwise noted.

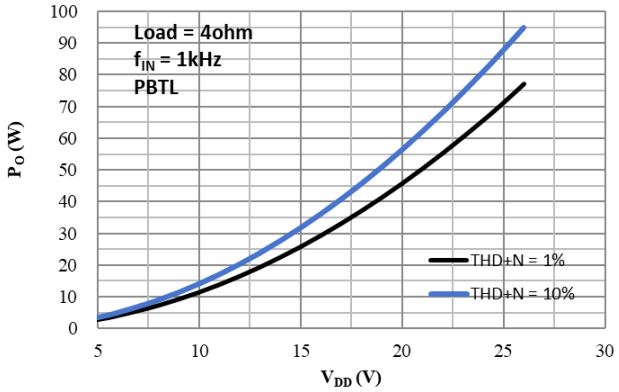
PV_{DD} vs I_{PVDD}



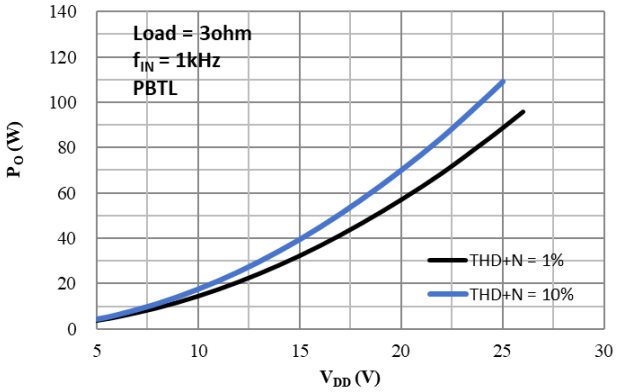
PV_{DD} vs I_{PVDD_SD}



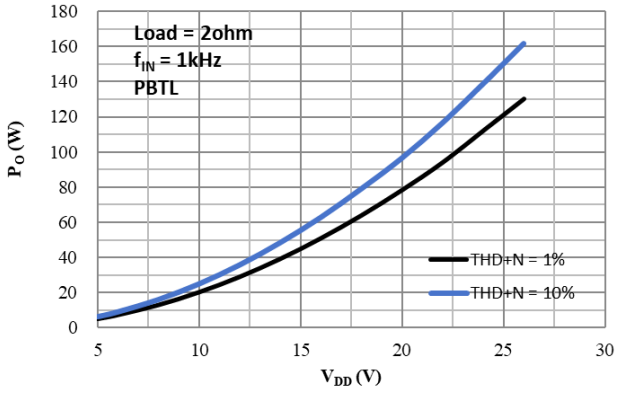
V_{DD} vs P_O



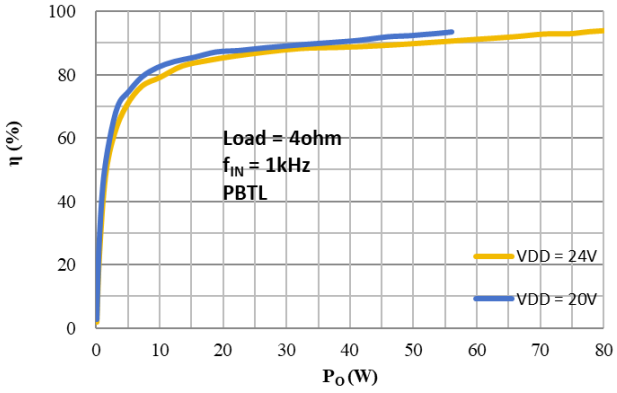
V_{DD} vs P_O

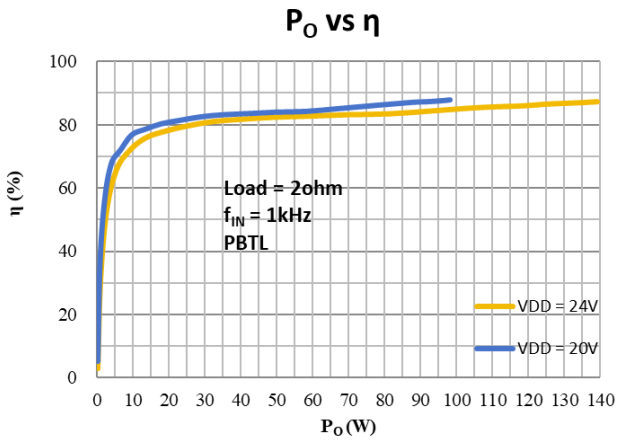


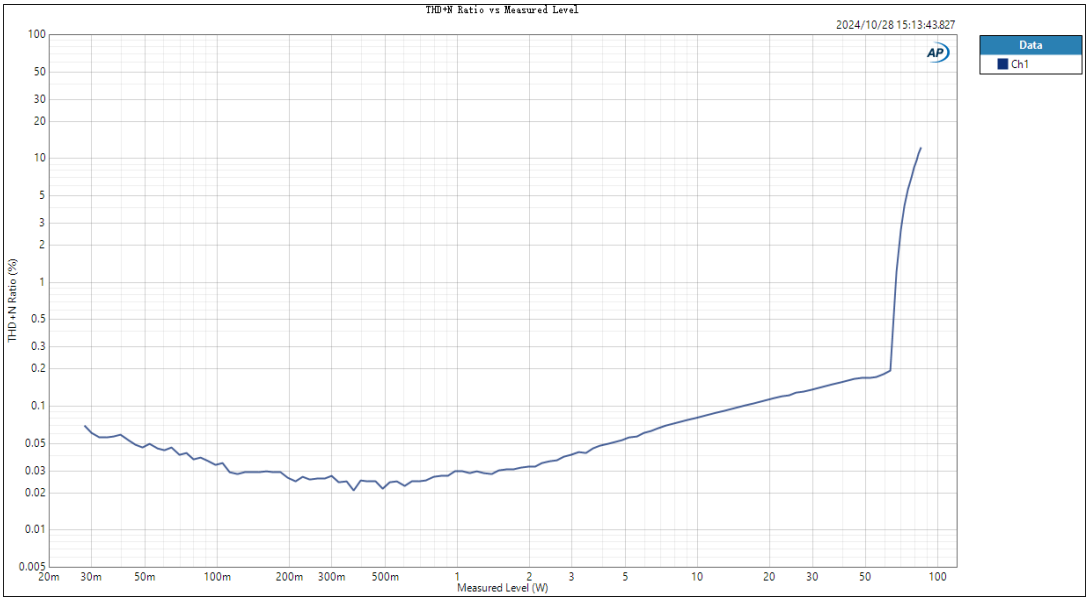
V_{DD} vs P_O



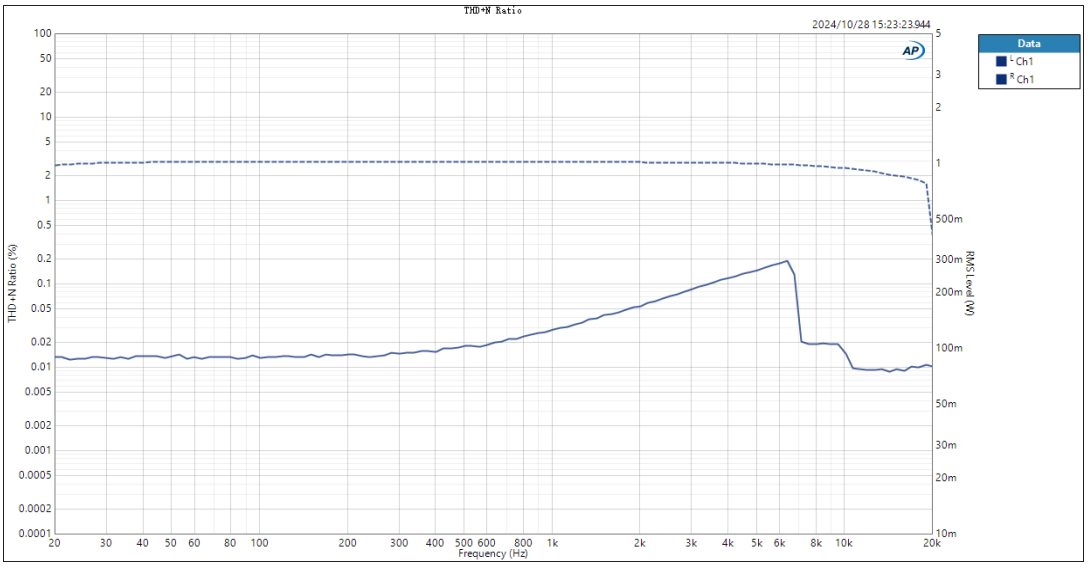
P_O vs η







THD+N vs Po, 24V, 4ohm



THD+N vs f_{IN}, 24V, 4ohm

■ APPLICATION INFORMATION

The HT5606 is a flexible and easy-to-use stereo class-D speaker amplifier with an I²S input serial audio port. The HT5606 supports a variety of audio clock configurations via two speed modes. In Hardware Control mode, the device only operates in single-speed mode. When used in I²C Control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2 kHz and 96 kHz. The outputs of the HT5606 can be configured to drive two speakers in stereo Bridge Tied Load (BTL) mode or a single speaker in Parallel Bridge Tied Load (PBTL) mode.

Only two power supplies are required for the HT5606. They are a 3.3-V power supply, called DVDD, for the small signal analog and digital and a higher voltage power supply, called PVDD for the output stage of the speaker amplifier and AVDD for analog power supply. To enable use in a variety of applications, PVDD can be operated over a large range of voltages, which is 4.5V – 26.4V, and it is recommended to put paralleled capacitor of 100nF//1uF//220uF between each channel of PVDD and system ground.

HT5606 是一颗简单易用且灵活的 I²S 数字输入 D 类音频功放，其具有两种速率模式，支持不同的采样频率。硬件模式下，器件工作在单倍速率模式；I²C 控制模式下，器件工作在双倍速率模式，可支持诸如 88.2 kHz 和 96 kHz 的采样频率。HT5606 的输出可配置成立体声双喇叭 BTL 输出，或单通道单喇叭 PBTL 输出。

HT5606 仅需要两种电源供电，即在 DVDD（数字电源）端加 3.3V，在 PVDD（功率电源）端加 4.5-26.4V。每个通道的 PVDD 端建议各加 100nF//1uF//220uF 的并联电容到地。

1 Speaker Amplifier Audio Signal Path

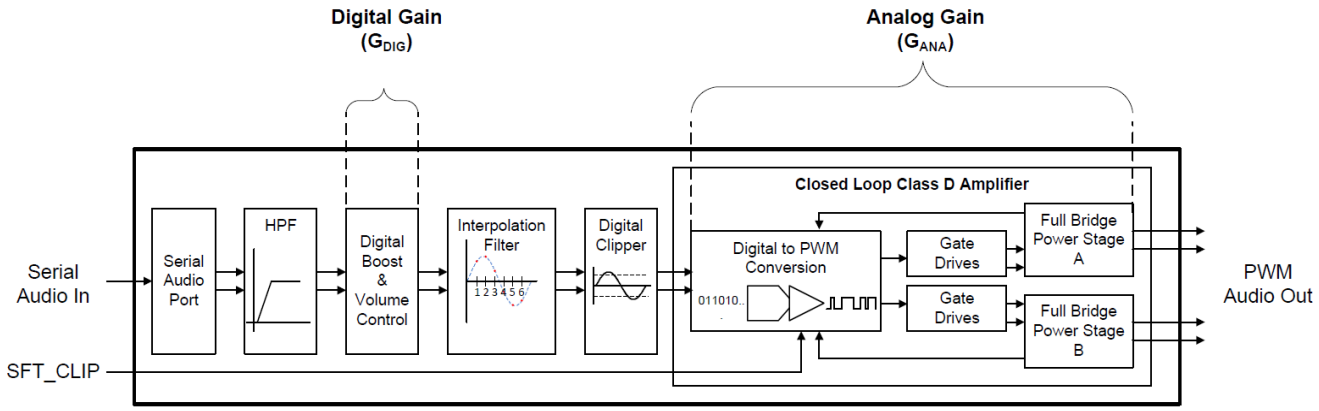


Figure 1 Speaker Amplifier Audio Signal Path

1.1 Serial Audio Port

The serial audio port (SAP) receives audio in either I²S, Left Justified, or Right Justified formats. In Hardware Control mode, the device operates only in 32, 48 or 64 × f_S I²S mode. In I²C Control mode, additional options for left-justified and right justified audio formats are available. The supported clock rates and ratios for Hardware Control Mode and I²C Control Mode are detailed in their respective sections below.

HT5606 的数字音频串行输入接口支持 I²S、左对齐、右对齐等数据格式。在硬件模式下，仅支持 32、48 或 64 × f_S I²S 输入。在软件模式下，还支持左对齐、右对齐的数据格式。具体如下。

1.1.1 I²S

I²S timing uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is LOW for the left channel and HIGH for the right channel. A bit clock, called SCLK, runs at 32, 48, or 64 × f_S and is used to clock in the data. There is a delay of one-bit clock from the time the LRCK signal changes state to the first bit of data on the data lines. The data is presented in 2's-complement form (MSB-first) and is valid on the rising edge of bit clock.

I² S 定时使用 LRCK 来定义传输的数据何时用于左通道，何时用于右通道。左声道的 LRCK 低，右声道的 LRCK 高。一个位时钟，称为 SCLK，以 32、48 或 64×f_S 的速率运行，用于同步数据。从 LRCK 信号改变状态到数据线上的第一位数据之间有一位时钟的延迟。数据以 2 的补码形式表示（MSB 优先），在位时钟上升沿有效。

1.1.2 Left-Justified

Left-justified (LJ) timing also uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is HIGH for the left channel and LOW for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time LRCK toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. The HT5606 can accept digital words from 16 to 24 bits wide and pads any unused trailing data-bit positions in the L/R frame with zeros before presenting the digital word to the audio signal path.

左对齐（LJ）使用 LRCK 来定义传输的数据何时用于左信道，何时用于右信道。左声道的 LRCK 高，右声道的 LRCK 低。一个位时钟，称为 SCLK，以 32、48 或 64×f_S 的速率运行，用于同步数据。在 LRCK 切换的同时，第一位数据出现在数据线上。数据首先写入 MSB，并且在位时钟的上升沿有效。HT5606 可以接受 16 到 24 位宽的数字字，在将数字字呈现给音频信号路径之前，用零填充 L/R 帧中任何未使用的尾随数据位位置。

1.1.3 Right-Justified

Right-justified (RJ) timing also uses LRCK to define when the data being transmitted is for the left channel and when it is for the right channel. LRCK is HIGH for the left channel and LOW for the right channel. A bit clock running at 32, 48, or 64 × f_S is used to clock in the data. The first bit of data appears on the data 8 bit-clock periods (for 24-bit data) after LRCK toggles. In RJ mode the LSB of data is always clocked by the last bit clock before LRCK transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The HT5606 pads unused leading data-bit positions in the left/right frame with zeros before presenting the digital word to the audio signal path.

右对齐（RJ）使用 LRCK 来定义传输的数据何时用于左通道，何时用于右通道。左声道的 LRCK 高，右声道的 LRCK 低。以 32、48 或 64×f_S 的速率运行的位时钟用于数据时钟。在 LRCK 切换后，第一位数据出现在数据 8 位时钟周期（对于 24 位数据）。在 RJ 模式下，数据的 LSB 总是在 LRCK 转换之前由最后一位时钟计时。数据首先写入 MSB，在位时钟上升沿有效。HT5606 在向音频信号路径呈现数字字之前，用零填充左/右帧中未使用的前导数据位位置。

1.2 DC Blocking Filter

Excessive DC content in the audio signal can damage loudspeakers and even small amounts of DC offset in the signal path cause audible artifacts when muting and unmuting the speaker amplifier. For these reasons, the amplifier employs two separate DC blocking methods for the speaker amplifier. The first is a high-pass filter provided at the front of the data path to remove any DC from incoming audio data before it is presented to the audio path. The –3 dB corner frequencies for the filter are specified in the speaker amplifier electrical characteristics table. In Hardware Control mode, the DC blocking filter is active and cannot be disabled. In software Control mode, the filter can be bypassed by writing a 1 to bit 6 of register 0x15. The second method is a DC detection circuit that will shut down the power stage if DC is found to be present on the output due to some internal error of the device. This DC Error (DCE) protection is discussed in the **DC Detect Protection** below.

音频信号持续的直流成分，可能损坏喇叭，或者产生输出直流偏置进而在静音/解除静音时产生噪声。因此，HT5606 具有两种隔直流的方式。

一种是在数据通道前端设置高通滤波器，以在数据输入端去除直流成分。该滤波器的截止频率已在上面参数表中列出。在硬件工作模式，该滤波器不能关闭；在软件控制模式，该滤波器可关闭（0x15 寄存器的 bit6）。

另一种是 DC 检测电路，当其检测到输出端有一定的直流成分的时候，HT5606 将关闭芯片。这种 DCE 保护将在下面 **DC Detect Protection** 描述。

1.3 Digital Boost and Volume Control

Following the high-pass filter, a digital boost block is included to provide additional digital gain if required for a given application as well as to set an appropriate clipping point for a given GAIN[1:0] pin configuration when in Hardware Control mode. The digital boost block defaults to +6dB when the device is in Hardware Mode. In most use cases, the digital boost block will remain unchanged when operating the device in I²C Control mode, as the volume control offers sufficient digital gain for most applications. The HT5606's digital volume control operates from Mute to 24 dB, in steps of 0.5 dB. The equation below illustrates how to set the 8-bit volume control register at address 0x13/0x14:

DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB])

Transitions between volume settings will occur at a rate of 0.5 dB every 8 LRCK cycles to ensure no audible artifacts occur during volume changes. This volume fade feature can be disabled via Bit 7 of Register 0x15.

在高通滤波隔直后是数字增益模块，该模块可为数字信号提供一个附加的数字增益，以适应不同的应用。在硬件模式下其默认设置是+6dB，并可在 I²C 控制模式下，通过寄存器修改。在大多数情况下，其设置后不用修改。

HT5606 的数字音量控制可通过 0x13 和 0x14 寄存器设置 Mute~+24dB（每步 0.5dB）。下面是如何设置该寄存器的公式：

DVC [Hex Value] = 0xCF + (DVC [dB] / 0.5 [dB])

数字音量的变化速率为 0.5dB/8LRCK，以避免音量突变产生噪声。这种音量渐变的功能可通过 0x15 寄存器的 bit7 关闭。

1.4 Digital Clipper

A digital clipper is integrated in the oversampled domain to provide a component-free method to set the clip point of the speaker amplifier. Through the "Digital Clipper Level x" (at register address 0x10, 0x11, 0x12) controls in the I²C control port, the point at which the oversampled digital path clips can be set directly, which in turns sets the 10% THD+N operating point of the amplifier. This is useful for applications in which a single system is designed for use in several end applications that have different power rating specifications. Its place in the oversampled domain ensures that the digital clipper is acoustically appealing and reduces or eliminates tones which would otherwise foldback into the audio band during clipping events. Figure 2 shows a block diagram of the digital clipper.

HT5606 集成了数字限幅器，无需任何元器件、仅通过寄存器（0x10, 0x11, 0x12）配置即可设置功放输出的削顶幅度，即功放 10% THD+N 工作点。其在一种硬件设计适应多种不同功率等级的应用终端时特别有用。下图 2 显示的是数字限幅器的模块图。

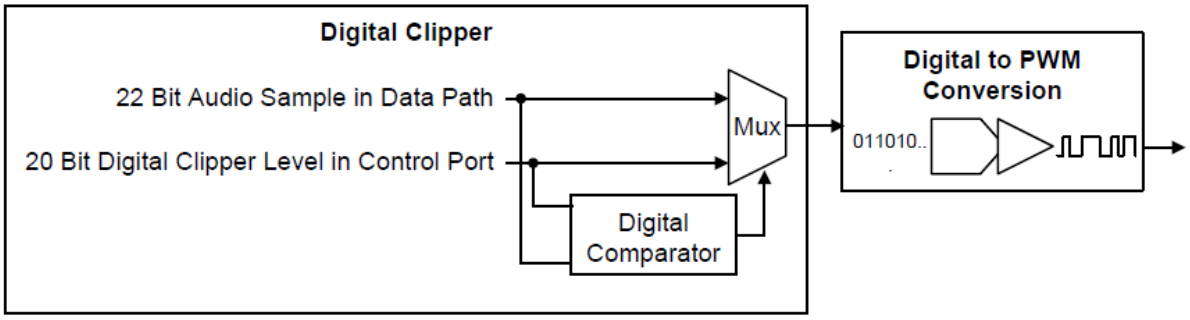


Figure 2 Digital Clipper Simplified Block Diagram

It is important to note that the actual signal developed across the speaker will be determined not only by the digital clipper, but also the analog gain of the amplifier. Depending on the analog gain settings and the PVDD level applied, clipping could occur as a result of the voltage swing that is determined by the gain being larger than the available PVDD supply rail. The gain structures are discussed in detail below for both Hardware Control Mode and I²C Control Mode.

需要了解的是，功放输出的最终幅度不止取决于该限幅器，还取决于当前设置的模拟增益和 PVDD 电压。增益设置将在下文讲述。

1.5 Closed-Loop Class-D Amplifier

Following the digital clipper, the interpolated audio data is next sent to the Closed-Loop Class-D amplifier, whose first stage is Digital to PWM Conversion (DPC) block. In this block, the stereo audio data is translated into two pairs of complimentary pulse width modulated (PWM) signals which are used to drive the outputs of the speaker amplifier. Feedback loops around the DPC ensure constant gain across supply voltages, reduce distortion, and increase immunity to power supply injected noise and distortion. The analog gain is also applied in the Class-D amplifier section of the device. The gain structures are discussed in detail below for both Hardware Control Mode and I²C Control Mode.

数字信号经过数字限幅器后，进入了闭环 D 类功放。D 类功放的第一级是数字转 PWM 模块（DPC），PWM 信号则被用来驱动功放输出级。DPC 的反馈环可保证恒定的增益，降低失真，提高对电源噪声的免疫力。该 D 类功放的模拟增益将在下文讲述。

The switching rate of the amplifier is configurable in both Hardware Control Mode and I²C Control Mode. In both cases, the PWM switching frequency is a multiple of the sample rate. This behavior is described in the respective Hardware Control Mode and I²C Control Mode sections below.

D 类功放的开关频率可通过硬件模式或 I²C 控制模式进行选择，具体将在下文讲述。

2 Speaker Amplifier Protection Suite

The speaker amplifier in the HT5606 includes a robust suite of error handling and protection features. It is protected against Over-Current, Under-Voltage, Over-Voltage, Over-Temperature, DC, and Clock Errors. The status of these errors is reported via the FAULT pin and the appropriate error status register in the I²C Control Port. The error or handling behavior of the device is characterized as being either "Latching" or "Non-Latching" depending on what is required to clear the fault and resume normal operation (that is playback of audio).

HT5606 具有多种保护功能，包括过流、欠压、过压、过温、DC、时钟错误等保护。这些故障将通过\FAULT 引脚和寄存器错误标志位反应。依据如何才能清除故障并恢复正常播放状态，这些故障被分类为"Latching"或"Non-Latching"两种类别。

Table. 1 Protection Suite Error Handling Summary

ERROR	CAUSE	FAULT TYPE	Error Is Cleared By
Overvoltage Error (OVE)	PVDD level rises above that specified by OVE_{RTH}	Non-latching	PVDD level returning below OVE_{FTH}
Undervoltage Error (UVE)	PVDD level drops below that specified by UVE_{RTH}	Non-latching	PVDD level returning above UVE_{RTH}
Clock Error (CLKE)	One or more of the following errors has occurred: 1. Non-supported MCLK to LRCK and/or SCLK to LRCK Ratio; 2. Non-supported MCLK or LRCK rate 3. MCLK, SCLK, or LRCK has stopped	Non-latching	Clocks returning to valid state
Overcurrent Error (OCE)	Speaker Amplifier output current has increased above the level specified by OCE_{TH}	Latching	\FAULT has passed AND \SD Pin or Bit Toggle
DC Detect Error (DCE)	DC offset voltage on the speaker amplifier output has increased above the level specified by the DCE_{TH}	Latching	\FAULT has passed AND \SD Pin or Bit Toggle
Overtemperature Error (OTE)	The temperature of the die has increased above the level specified by the OTE_{TH}	Latching	\FAULT has passed AND \SD Pin or Bit Toggle AND the temperature of the device has reached a level below that which is dictated by the OTE_{HYS} specification

For latching errors, the \SD pin or the SD bit in the control port must be toggled in order to clear the error and resume normal operation. If the error is still present when the \SD pin or SD bit transitions from LOW back to HIGH, the device will again detect the error and enter into a fault state resulting in the error status bit being set in the control port and the \FAULT line being pulled LOW. If the error has been cleared (for example, the temperature of the device has decreased below the error threshold) the device will attempt to resume normal operation after the \SD pin or SD bit is toggled and the required fault time out period (T_{FAULT}) has passed. If the error is still present, the device will once again enter a fault state and must be placed into and brought back out of shutdown in order to attempt to clear the error.

For non-latching errors, the device will automatically resume normal operation (that is playback) once the error has been cleared. The non-latching errors, with the exception of clock errors will not cause the \FAULT line to be pulled LOW. It is not necessary to toggle the \SD pin or SD bit in order to clear the error and resume normal operation for non-latching errors. Table. 1 details the types of errors protected by the HT5606's Protection Suite and how each are handled.

对于latching故障，\SD引脚或bit位SD必须进行切换，从而清除故障，使芯片恢复正常工作状态。如果该故障仍存在，当\SD引脚或bit位SD从低到高时，器件会重新监测到故障，从而再次进入故障状态，对应寄存器标志位进行错误标志，\FAULT被拉低。如果故障被清除（例如器件温度下降至故障阈值以下），器件将在\SD引脚或bit位SD切换后T_{FAULT}时间恢复正常工作状态。如果该故障仍存在，芯片将重新进入错误状态，必须先将芯片进入关断模式、再退出关断模式，芯片才会试图清除错误。

对于 Non-Latching 故障，当故障清除时，器件将自动恢复到工作状态。这类故障中，除了时钟错误，其他均不会导致\FAULT 引脚拉低。对于这类故障，不需要动作\SD 引脚或 bit 位 SD，芯片即可恢复正常工作。表 1 对这些故障进行了详细的说明。

2.1 \FAULT pin

In both hardware and I²C Control mode, the \FAULT pin of the HT5606 serves as a fault indicator to notify the system that a fault has occurred with the speaker amplifier by being actively pulled LOW. This pin is an open-drain output pin and, unless one is provided internal to the receiver, requires an external pullup to set the net to a known value. The behavior of this pin varies based upon the type of error which has occurred.

In the case of a latching error, the fault line will remain LOW until such time that the HT5606 has resumed normal operation (that is the \SD pin has been toggled and T_{FAULT} has passed).

With the exception of clock errors, non-latching errors will not cause the \FAULT pin to be pulled LOW. Once a non-latching error has been cleared, normal operation will resume. For clocking errors, the \FAULT line will be pulled LOW, but upon clearing of the clock error normal operation will resume automatically, that is, with no T_{FAULT} delay.

One method which can be used to convert a latching error into an auto-recovered, non-latching error is to connect the \FAULT pin to the \SD pin. In this way, a fault condition will automatically toggle the \SD pin when the \FAULT pin goes LOW and returns HIGH after the \FAULT period has passed.

在硬件工作模式和 I²C 控制模式，HT5606 的\FAULT 脚作为故障显示，当芯片发生故障时，该引脚拉低。该引脚是开漏结构的输出脚，需要在外部通过电阻上拉至固定电平，或连接至主控 I/O。

对于 latching 故障，\FAULT 脚将保持为低，直至芯片进入正常工作状态（即\SD 已切换且经过了 T_{FAULT} 时间）。

对于 non-latching 故障，除了时钟错误，其他均不会导致\FULAT 脚拉低。一旦这类故障被清除，芯片将进入正常工作状态。对于时钟错误，\FAULT 引脚被拉低，故障清除后，芯片同样可立即进入正常工作状态。

当\FAULT 脚连接至\SD 脚，latching 故障可转化为可自动恢复的 non-latching 故障，此时，故障可通过\FAULT 脚拉低，将\SD 脚从高电平到低电平切换，并在 T_{FAULT} 后\SD 恢复高。

2.2 DC Detect Protection

The HT5606 has circuitry which will protect the speakers from DC current which might occur due to an internal amplifier error. The device behavior in response to a DCE event is detailed in the table in the previous section.

A DCE event occurs when the output differential duty-cycle of either channel exceeds 60% for more than 420 msec at the same polarity. The table below shows some examples of the typical DCE Protection threshold for several values of the supply voltage. This feature protects the speaker from large DC currents or AC currents less than 2 Hz.

The minimum output offset voltages required to trigger the DC detect are listed in Table. 2. The outputs must remain at or above the voltage listed in the table for more than 420 msec to trigger the DC detect.

HT5606具有DC直流保护，以保护扬声器。芯片产生直流保护时，\FAULT拉低，功放输出切换到高阻状态。经过t_{FAULT}时间后，芯片将自动尝试恢复，若故障已消失，芯片恢复；若故障仍在，芯片再次进入保护状态。

当功放任一通道相同极性的输出差分占空比超过 60%且保持 420ms 以上时，DC 直流保护触发。此功能用以在大电流直流和低于 2Hz 的 AC 电流时保护喇叭。

触发 DC 检测的最小输出偏置电压，如下表 2 所示。输出必须保持或高于下表电压并持续 420ms 才会触发直流监检测。

Table. 2 DC Detect Threshold

PVDD (V)	|Vos| (V)
4.5	0.96
6	1.3
12	2.6
18	3.9

2.3 Foldback (TFB) Function

The HT5606 Thermal Foldback, TFB, is designed to protect the HT5606 from excessive die temperature in case of the device being operated beyond the recommended temperature or power limit, or with a weaker thermal system than recommended, without shutting the device down. In hardware control mode, it's enabled by default. In I²C control mode, the function can be disabled through bit 4 register of 0x00.

The TFB works by reducing the on die power dissipation by reducing the HT5606 system gain by the rate of attack time (default value 1200ms/dB, can be modified in register address 0x00 in I²C control mode) by 0.25dB per step (step pace, which can be modified at bit 6 of register 0x00 in I²C control mode) if the TFB trig point is exceeded. Once the die temperature drops below the TFB trig point, the HT5606 gain is increased by a single or by the rate of release time (default value 2400ms/dB, can be modified in register address 0x00 in I²C control mode) by 0.25dB per step (step pace, which can be modified at bit 6 of register 0x00 in I²C control mode) until the TFB trig point, or a maximum attenuation is reached, and the system gain will be decreased again, or the system gain is at its nominal gain level. The procedure shows as follows.

HT5606 限温控制功能 TFB，设计用于保护 HT5606 免受芯片温度过高的影响，当器件在过高的环境温度、较大的功率输出、较差的板级热性能条件下，不至于芯片关闭，仍能保持一定的功率输出。在硬件控制模式下，它默认启用。在 I²C 控制模式下，可通过 0x00 的第 4 位寄存器禁用该功能态。

TFB 的工作原理是，如果超过 TFB 触发点，则以启动时间（默认值 1200ms/dB，可在 I2C 控制模式下的寄存器地址 0x00 中修改）的速率控制 HT5606 系统增益降低，0.25dB/步（步长，可在 I2C 控制模式下的寄存器 0x00 的位 6 处修改）以降低芯片功耗。一旦芯片温度降到 TFB 触发点以下，则以释放时间（默认值 2400ms/dB，可在 I2C 控制模式下的寄存器地址 0x00 中修改）的速率增加 HT5606 增益， 0.25dB/步（步长，可在 I2C 控制模式下的寄存器 0x00 的位 6 处修改），直到 TFB 触发点，或者达到最大增益增加极限，系统增益将再次降低，或者系统增益处于其正常增益水平。过程如下所示。

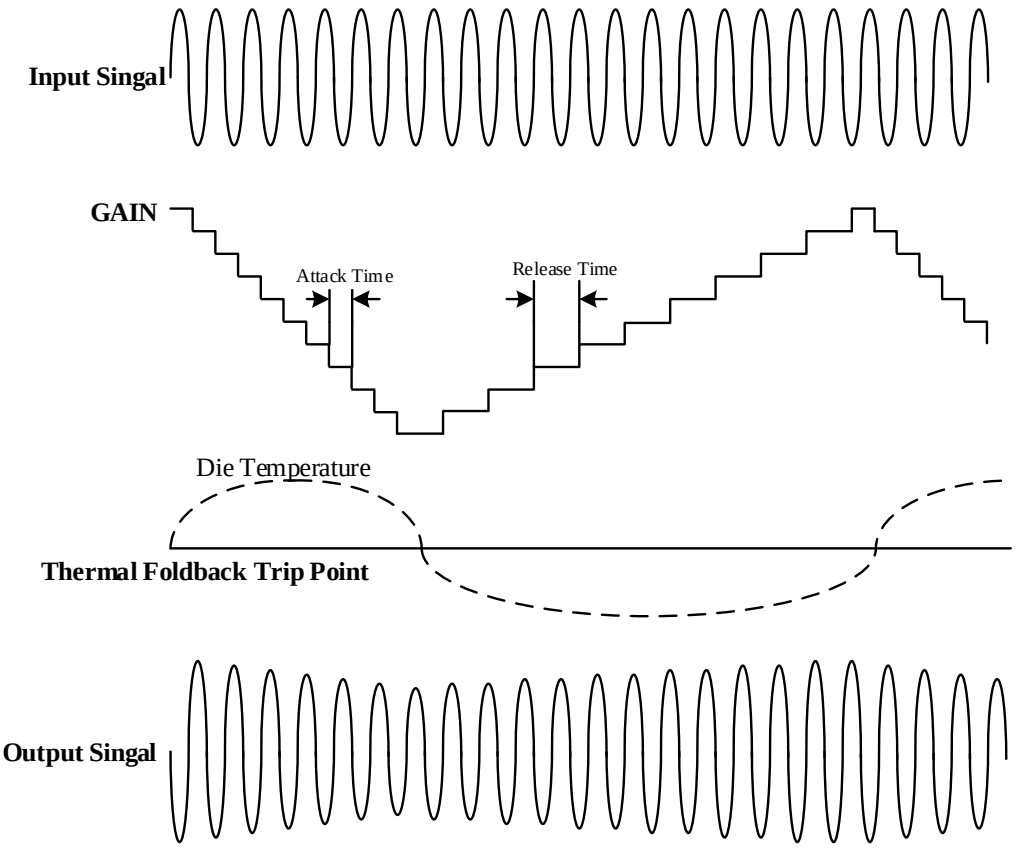


Figure 3 TFB Operation

3 Device Functional Modes

3.1 Hardware Control Mode

For systems which do not require the added flexibility of the I²C control port or do not have an I²C host controller, the HT5606 can be used in Hardware Control Mode. In this mode of operation, the device operates in its default configuration and any changes to the device are accomplished via the hardware control pins, described below. The audio performance between Hardware and I²C Control mode is identical, however more features and functionality are available when the device is operated in I²C Control mode. The behavior of these Hardware Control Mode pins is described in the sections below.

对于不需要增加 I²C 控制端口灵活性或没有 I²C 主机控制器的系统，HT5606 可以在硬件控制模式下使用。在这种操作模式下，设备以其默认配置运行，对设备的任何更改都通过硬件控制引脚完成。硬件和 I²C 控制模式之间的音频性能是相同的，但是当设备在 I²C 控制模式下运行时，可以获得更多的特性和功能。硬件控制模式下的引脚说明将在下文描述。

Several static I/O's are present on the HT5606 which are meant to be configured during PCB design and not changed during normal operation. Some examples of these are the GAIN[1:0] and PBTL/SCL pins. These pins are often referred to as being tied or pulled LOW or tied or pulled HIGH. A pin which is tied or pulled LOW has been connected directly to the system ground. The HT5606 is configured such that the most popular use cases for the device (that is BTL mode, 384-kHz switching frequency, and so forth) require the static I/O lines to be tied LOW. This ensures optimum thermal performance as well as BOM reduction.

HT5606 上存在多个静态 I/O，这些 I/O 在 PCB 设计期间配置，在正常工作期间不会改变。比如 GAIN[1:0]和 PBTL/SCL 引脚。对于最常用的设置（即 BTL 模式、384kHz 开关频率等），HT5606 的相关静态 I/O 为拉低，其可直接接至系统地。

Device pins that need to be tied or pulled HIGH should be connected to DVDD. For these pins, a pull-up resistor is recommended to limit the slew rate of the voltage which is presented to the pin during power up. Depending on the output impedance of the supply, and the capacitance connected to the DVDD net on the board, slew rates of this node could be high enough to trigger the integrated ESD protection circuitry at high current levels, causing damage to the device.

需要拉高的引脚应连接到 DVDD。对于这些引脚，建议使用上拉电阻器来限制上电期间提供给引脚的电压上升斜率。

3.1.1 Speaker Amplifier Shut Down (\SD pin)

In both Hardware and I²C Control mode, the \SD pin is provided to place the speaker amplifier into shutdown. Driving this pin LOW will place the device into shutdown, while pulling it HIGH (to DVDD) will bring the device out of shutdown. This is the lowest power consumption mode that the device can be placed in while the power supplies are up. If the device is placed into shutdown while in normal operation, an audible artifact may occur on the output.

在硬件模式和 I²C 控制模式下，\SD 引脚均作为关断芯片的使能脚，当其拉低时，芯片进入关断模式；当其拉高至 DVDD 时，芯片退出关断模式。在关断模式下，芯片进入最低功耗状态。芯片从正常工作状态切入关断模式时，可闻 pop 声会产生在输出端。

It is recommended that the duration between 2 actions of Shut Down should be more than 10 msec.

另外建议，两次关断之间间隔不能小于 10ms。

3.1.2 Serial Audio Port in Hardware Control Mode

When used in Hardware Control Mode, the Serial Audio Port (SAP) accepts only I²S formatted data. Additionally, the device operates in Single-Speed Mode (SSM), which means that supported sample rates, MCLK rates, and SCLK rates are limited to those shown in the table below. Additional clocking options, including higher sample rates, are available when operating the device in I²C Control Mode.

Table. 3 details the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK rate, the supported SCLK rates are shown and are represented in multiples of the sample rate, which is written as "× f_S".

硬件控制模式下，串行音频端口（SAP）仅接受 I² S 格式的数据。此外，该器件以单速模式（SSM）运行，这意味着支持的采样率、MCLK 速率和 SCLK 速率仅限于下表所示的速率。在 I²C 控制模式下操作器件时，还更高的采样率。

表 3 详细说明每个可用采样率和 MCLK 速率配置支持的 SCLK 速率。对于每个 f_S 和 MCLK 速率，支持的 SCLK 速率显示在表中，并以采样率的倍数表示，该比率写为“×f_S”。

Table. 3 Supported SCLK rates in hardware control mode (Single speed mode)

Sample Rate fs (kHz)	**MCLK rate (× fs)**				
	128	192	256	384	512
	SCLK rate (× fs)				
12	N/S	N/S	N/S	N/S	32, 48, 64
16	N/S	N/S	32, 48, 64	32, 48, 64	32, 48, 64
24	N/S	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
32	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
38	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
44.1	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64
48	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64	32, 48, 64

3.1.3 Speaker Amplifier Switching Frequency Select (FREQ/SDA)

In Hardware Control mode, the PWM switching frequency of the HT5606 is configurable via the FREQ/SDA pin. When connected to the system ground, the pin sets the output switching frequency to 8 × f_S. When connected to DVDD through a pull-up resistor, the pin sets the output switching frequency to 16 × f_S. More switching frequencies are available when the HT5606 is used in I²C Control Mode. Please notice that a switching frequency between 300kHz and 600kHz will get a better performance for the Class D amplifier. For example, an output switching frequency of 8 × f_S is recommended when 48kHz fs is used. Detailed recommendations for the FREQ selection are listed in Table. 7 Recommendations for the FREQ Selection.

在硬件控制模式下，HT5606 的 PWM 开关频率可通过 FREQ/SDA 引脚配置。当其连接到系统地时，开关频率设置为 8×f_S。当其通过上拉电阻器连接到 DVDD 时，输出开关频率设置为 16×f_S。当 HT5606 用于 I²C 控制模式时，可以使用更多的开关频率。请注意，在 300kHz 和 600kHz 之间的开关频率将为 D 类放大器提供更好的性能。例如，当使用 48kHz f_S 时，建议输出开关频率为 8×f_S。表 8 中列出了频率选择的详细建议。

3.1.4 Parallel Bridge Tied Load Mode Select (PBTL/SCL pin)

The HT5606 can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the output impedance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of current the speaker amplifier can source before hitting the over-current error threshold.

The device can be placed operated in PBTL mode in either Hardware Control Mode or in I²C Control Mode.

To place the HT5606 into PBTL Mode when operating in Hardware Control Mode, the PBTL/SCL pin should be pulled HIGH (that is, connected to the DVDD supply through a pull-up resistor). If the device is to operate in BTL mode instead, the PBTL/SCL pin should be pulled LOW, that is connected to the system supply ground. When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

HT5606 可以配置为驱动两个输出通道并联的单个扬声器。这种运行模式称为并行桥接（PBTL）模式。这种工作模式有效地将放大器的输出阻抗降低了一半，进而降低了由于通过输出 FET 的传导损耗而在器件中耗散的功率。此外，由于输出通道是并行工作的，因此在达到过流关断阈值之前，它还将功放可以提供的电流量增加一倍。

该器件可以在硬件控制模式或 I²C 控制模式下置于 PBTL 模式下运行。

在硬件控制模式时，要将 HT5606 置于 PBTL 模式，应将 PBTL/SCL 引脚拉高（即通过上拉电阻器连接到 DVD 电源）。如果设备在 BTL 模式下工作，则 PBTL/SCL 引脚应拉低，即连接到系统电源接地。在 PBTL 模式下工作时，输出引脚应按照典型应用电路图所示进行连接。

In PBTL mode, the amplifier selects its source signal from the right channel of the stereo signal presented on the SDIN line of the Serial Audio Port. To select the left channel of the stereo signal, the LRCK can be inverted in the processor that is sending the serial audio data to the HT5606, or the bit7 of register 0x16 can be changed into 0.

在 PBTL 模式下，放大器从串行音频端口的 SDIN 线上显示的立体声信号的右声道选择其源信号。要选择立体声信号的左声道，可以在向 HT5606 发送串行音频数据的处理器中反转 LRCK，也可以在寄存器 0x16 的 Bit7 中修改。

3.1.5 Speaker Amplifier Sleep Enable (SLEEP/ADR pin)

In Hardware Control mode, pulling the SLEEP/ADR pin HIGH gracefully transitions the switching of the output devices to a non-switching state or "High-Z" state. This mode of operation is similar to mute in that no audio is present on the outputs of the device. However, unlike the 50/50 mute available in the I²C Control Port, sleep mode saves quiescent power dissipation by stopping the speaker amplifier output transistors from switching. This mode of operation saves quiescent current operation but keeps signal path blocks active so that normal operation can resume more quickly than if the device were placed into shutdown.

在硬件控制模式下，将 SLEEP/ADR 引脚拉高可以将芯片的输出切换为高阻状态，其类似于 MUTE 静音状态，即无音乐输出。但是，与 I²C 寄存器中提供的 50/50 静音不同，睡眠模式通过停止扬声器放大器输出晶体管的切换来节省静态功耗。这种操作模式节省了静态电流操作，但使信号路径块保持激活状态，以便恢复正常操作的速度比关闭设备时更快。

3.1.6 Gain Setting

In Hardware Control Mode, a combination of digital gain and analog gain is used to provide the overall gain of the speaker amplifier. The decode of the two pins "GAIN1" and "GAIN0" sets the gain of the speaker amplifier. Additionally, pulling both of the GAIN[1:0] pins HIGH places the device into I2C control mode.

As seen in Figure 4, the audio path of the HT5606 consists of a digital audio input port, a digital audio path, a digital to PWM converter (DPC), a gate driver stage, a Class D power stage, and a feedback loop which feeds the output information back into the DPC block to correct for distortion sensed on the output pins. The total amplifier gain is comprised of digital gain, shown as G_{DIG} in the digital audio path and the analog gain from the input of the analog modulator G_{ANA} to the output of the speaker amplifier power stage.

在硬件控制模式下，使用数字增益和模拟增益的组合来提供扬声器放大器的整体增益。芯片是通过两个引脚“GAIN1”和“GAIN0”来设置功放的增益。此外，将两个 GAIN[1:0]引脚拉高会将设备置于 I²C 控制模式。

如图 8 所示，HT5606 的音频路径由数字音频输入端口、数字音频路径、数字到 PWM 转换器（DPC）、栅极驱动器级、D 类功率级和反馈回路组成，反馈回路将输出信息反馈回 DPC 块，以校正输出引脚上检测到的失真。放大器总增益由数字音频路径中数字增益（G_{DIG}）和模拟增益（G_{ANA}）益组成。

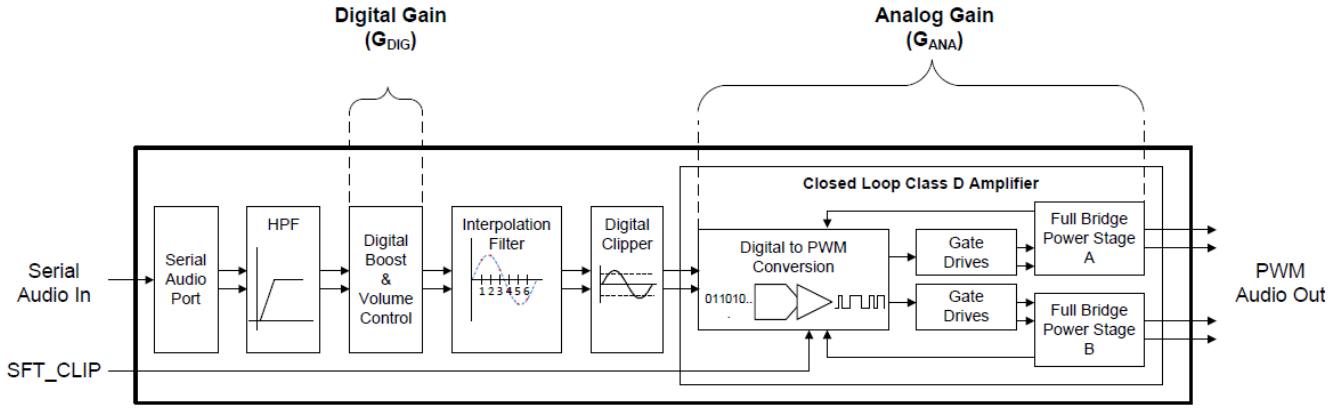


Figure 4 Speaker Amplifier Gain Select

As shown in Figure 4, the first gain stage for the speaker amplifier is present in the digital audio path. It consists of the volume control and the digital boost block. The volume control is set to 0dB by default and, in Hardware Control mode, it does not change. For all settings of the GAIN[1:0] pins, the digital boost block remains at +6 dB as analog gain block is transitioned through 19.2, 22.6, and 25 dB.

The values of G_{DIG} and G_{ANA} for each of the GAIN[1:0] settings are shown in the table below.

如图 8 所示，扬声器放大器的第一级增益出现在数字音频路径中。它由音量控制和数字升压模块组成。音量控制默认设置为 0dB，在硬件控制模式下，它不会更改。对于 GAIN[1:0]引脚的所有设置，即在模拟增益为 19.2、22.6 和 25 dB 时，数字升压模块均保持在+6 dB。

GAIN[1:0]设置对应的 G_{DIG} 和 G_{ANA} 值如下表所示。

Table. 4 Gain Structure for Hardware Control Mode

GAIN[1:0] pin Setting	Volume Control (dB)	Digital Boost (dB)	Analog Gain (dB)	Total System Gain (dB)
00	0	6	19.2	25.2
01	0	6	22.6	28.6
10	0	6	25	31
11	I²C Control Mode, Gain is controlled via I²C Port			

3.2 I²C Control Mode

In order to place the device in I²C control mode, the two gain pins (GAIN[1:0]) should be pulled HIGH. When this is done, the PBTL/SCL and FREQ/SDA pins are allocated to serve as the clock and data lines for the I²C Control Port.

为了将设备置于 I²C 控制模式，应将两个增益引脚（GAIN[1:0]）拉高。完成此操作后，PBTL/SCL 和 FREQ/SDA 引脚被分配用作 I² C 控制端口的时钟和数据线。

3.2.1 Speaker Amplifier Shut Down (\SD pin)

In both hardware and I²C Control mode, the \SD pin is provided to place the speaker amplifier into shutdown. The configuration is detailed in section 3.1.1.

在硬件模式和 I²C 控制模式下，\SD 引脚均作为关断芯片的使能脚，其设置同 3.1.1。

3.2.2 Serial Audio Port Controls

In I²C Control mode, additional digital audio data formats and clock rates are made available via the I²C control port. With these controls, the audio format can be set to left justified, right justified, or I²S formatted data.

When used in I²C Control mode, the device can be placed into double speed mode to support higher sample rates, such as 88.2 kHz and 96 kHz. Set register 0x15 bit3 SS/DS to 1 into higher sample rate. The tables below detail the supported SCLK rates for each of the available sample rate and MCLK rate configurations. For each f_S and MCLK Rate the support SCLK rates are shown and are represented in multiples of the sample rate, which is written as "x f_S".

在 I²C 控制模式下，通过 I²C 控制端口提供更多的数字音频数据格式和时钟速率，可以将音频格式设置为左对齐、右对齐或 I²S 格式的数据。

在 I²C 控制模式下，器件可置于双速模式，以支持更高的采样率，如 88.2 kHz 和 96 kHz。将寄存器 0x15 bit3 SS/DS 设置为 1 以获得更高的采样率。下表详细说明了每个可用采样率和 MCLK 速率配置支持的 SCLK 速率，并以采样速率的倍数表示，该倍数写为“x f_S”。

Table. 5 Supported SCLK rates in Double speed mode

Sample Rate fs (kHz)	MCLK rate (× fs)		
	128	192	256
	SCLK rate (× fs)		
88.2	32, 48, 64	32, 48, 64	32, 48, 64
96	32, 48, 64	32, 48, 64	32, 48, 64

3.2.3 Parallel Bridge Tied Load Mode (PBTL)

The HT5606 can be configured to drive a single speaker with the two output channels connected in parallel. This mode of operation is called Parallel Bridge Tied Load (PBTL) mode. This mode of operation effectively reduces the on resistance of the amplifier in half, which in turn reduces the power dissipated in the device due to conduction losses through the output FETs. Additionally, since the output channels are working in parallel, it also doubles the amount of current the speaker amplifier can source before hitting the over-current error threshold.

It should be noted that the device can be placed operated in PBTL mode in either Hardware Control Mode or in I2C Control Mode. For instructions on placing the device in PBTL via the BTL/SCL Pin, see Hardware Control Mode.

To place the HT5606 into PBTL Mode when operating in I2C Control Mode, the Bit 3 of Register (0x04) should be set in the control port. This bit is cleared by default to configure the device for BTL mode operation. An additional control available in I2C mode control is PBTL Channel Select, which elects which of the two channels presented on the SDIN line will be used for the input signal for the amplifier. This is found at Bit 7 of (0x16). When operated in PBTL mode, the output pins should be connected as shown in the Typical Application Circuit Diagrams.

It is important that before power supplies are brought up, \SD pin should be pulled low. Only after I2C register is programed (including PBTL register), \SD pin can be pulled high.

HT5606 可以配置为驱动两个输出通道并联的单个扬声器。这种运行模式称为并行桥接（PBTL）模式。这种工作模式有效地将放大器的导通电阻降低了一半，进而降低了由于通过输出 FET 的传导损耗而在器件中耗散的功率。此外，由于输出通道是并行工作的，因此在达到过流保护阈值之前，它还将扬声器放大器可以提供的电流量增加一倍。

应该注意的是，设备可以在硬件控制模式或 I²C 控制模式下置于 PBTL 模式下运行。有关通过 BTL/SCL 引脚将设备置于 PBTL 的说明，请参阅硬件控制模式。

在 I2C 控制模式下运行时，要将 HT5606 置于 PBTL 模式，应在控制端口中设置寄存器（0x04）的第 3 位。默认情况下，此位被清除，以将设备配置为 BTL 模式操作。I²C 模式控制中的一个附加控制是 PBTL 通道选择，它选择 SDIN 线路上显示的两个通道中的哪个将用于放大器的输入信号。其位于（0x16）的第 7 位。在 PBTL 模式下工作时，输出引脚应按典型应用电路图所示进行连接。

重要的是，在启动电源之前，\SD 引脚应拉低。只有对 I²C 寄存器（包括 PBTL 寄存器）进行配置后，\SD 引脚才能被拉高。

3.2.4 Speaker Amplifier Gain

As detailed in section 3.1.7, the speaker amplifier gain includes the analog gain and digital gain, both are configured directly in registers when operating in I²C Control mode. It is important to note that the digital boost block is separate from the volume control. The digital boost block should be set before the speaker amplifier is brought out of mute and not changed during normal operation. In most cases, the digital boost can be left in its default configuration, and no further adjustment is necessary.

如第 3.1.7 节所述，扬声器放大器增益包括模拟增益和数字增益，在 I²C 控制模式下运行时，这两种增益都直接在寄存器中配置。重要的是要注意，数字增益提升模块是独立于音量控制的。数字增益提升模块应在扬声器放大器退出静音状态之前设置，并且在正常操作期间不得更改。在大多数情况下，数字增益提升模块可以保留在其默认配置，无需进一步调整。

3.3 I²C Control Port

3.3.1 I²C Device Address

Each device on the I²C bus has a unique address that allows it to appropriately transmit and receive data to and from the I²C master controller. As part of the I²C protocol, the I²C master broadcast an 8-bit word on the bus that contains a 7-bit device address in the upper 7 bits and a read or write bit for the LSB. The HT5606 has a configurable I²C address. The SLEEP/ADR can be used to set the device address of the HT5606. In I²C Control mode, the seven bit I²C device address is configured as "110110x[R/W]", where "x" corresponds to the state of the SLEEP/ADR pin at first power up sequence of the device. If the SLEEP/ADR pin is tied LOW at power up, the device address will be set to 1101100[R/W]. If it is pulled HIGH, the address will be set to 1101101[R/W] at power up.

每个器件在 I²C 总线上具有一个唯一的器件地址，以便正确的将数据传输至 I²C 主机及从 I²C 主机接收数据。作为 I² C 协议的一部分，I²C 主机在总线上广播一个 8 位字节的地址，该字节包含高 7 位的 7 位设备地址和 LSB 的读或写位。HT5606 通过引脚 SLEEP/ADR 可设置 I²C 地址，"110110x[R/W]"，其中"x"对应于设备第一次通电时的 SLEEP/ADR 引脚状态。如果 SLEEP/ADR 引脚在上电时是拉低的，则器件地址将设置为 1101100[R/W]。如果被拉高，则为 11011001[R/W]。

3.3.2 General Operation of the I²C Control Port

The HT5606 device has a bidirectional I²C interface that is compatible with the Inter IC (I²C) bus protocol and supports both 100-kHz and 400-kHz data transfer rates. This is a slave-only device that does not support a multi-master bus environment or wait-state insertion.

HT5606 I²C 接口支持双向传输，该接口与 I²C 总线协议兼容，并支持 100 kHz 和 400 kHz 数据传输速率。这是一个从设备，不支持多主机的总线环境，及等待状态下的插入。

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period.

I²C 总线具有两个信号，SDA（数据）和 SCL（时钟），在系统中的器件之间使用串行数据传输进行通信。地址和数据的 8 位字节首先传输最高有效位（MSB）。此外，总线上传输的每个字节由接收设备用确认位（ACK）进行确认。每个传输操作从主设备驱动总线上的启动条件开始，并以主设备驱动总线上的停止条件结束。当时钟处于逻辑高电平时，总线使用数据终端（SDA）上的转换来指示启动和停止条件。SDA 上的高到低转换表示开始，低到高转换表示停止。正常的数据位转换必须在时钟为低时发生。

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

主机生成 7 位从机地址和读/写（R/W）位，以打开与另一个设备的通信，然后等待确认条件。在应答时钟周期内，设备保持 SDA 低，以指示确认。当发生这种情况时，主机发送序列的下一个字节。每个设备有唯一的 7 位从机地址加上 R/W 位（1 字节）。所有兼容设备通过并联的总线共享信息。

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Use pull-up resistors between 4.7 kΩ and 10 kΩ for SCL for a suitable rise time, as an internal serial resistor around 1.2kΩ is placed.

SDA 和 SCL 需通过外部上拉电阻截至逻辑高电平。SCL 上拉电阻使用 4.7kΩ~10kΩ 以获得合适上升沿时间，因其内部有约 1.2kΩ 的串联电阻。

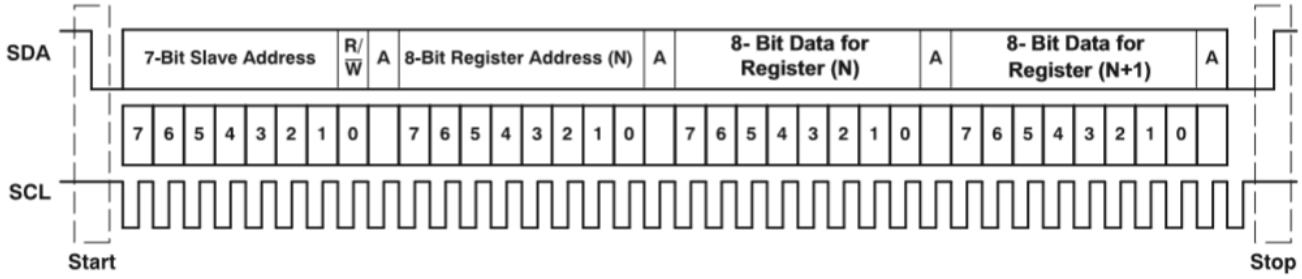


Figure 5 Typical I²C Sequence

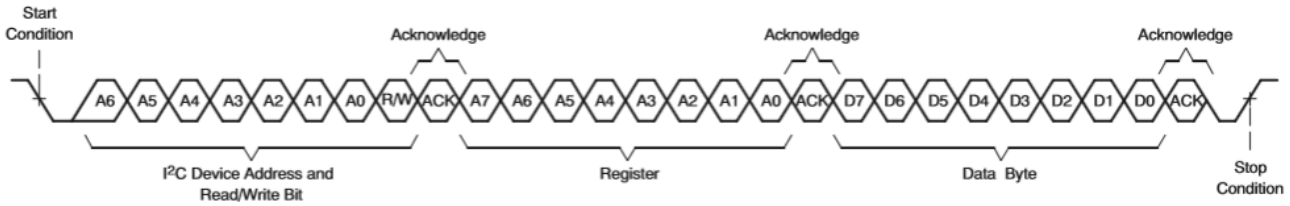


Figure 6 Single-Byte Write Transfer

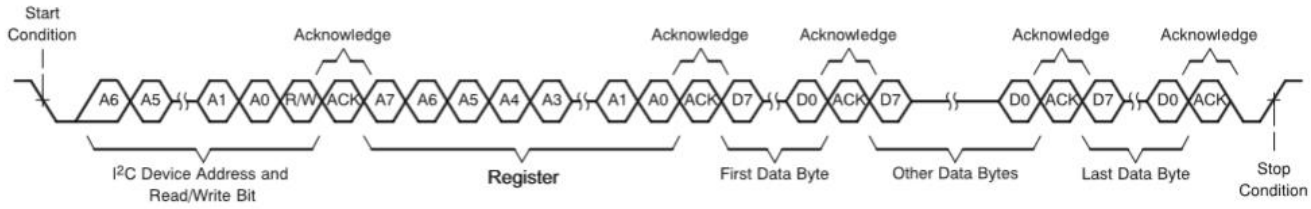


Figure 7 Multiple-Byte Write Transfer

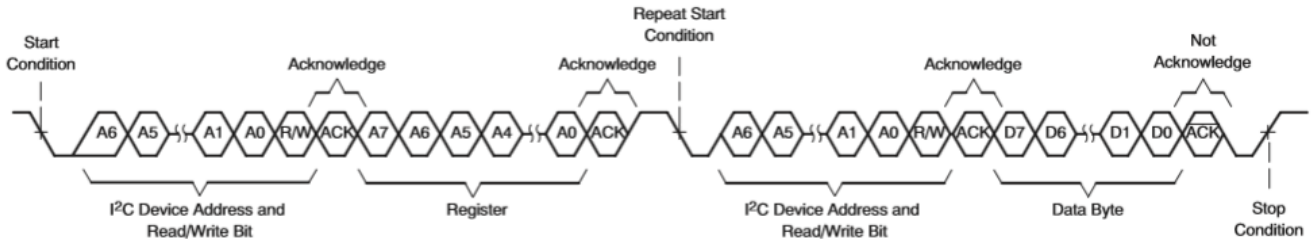


Figure 8 Single-Byte Read Transfer

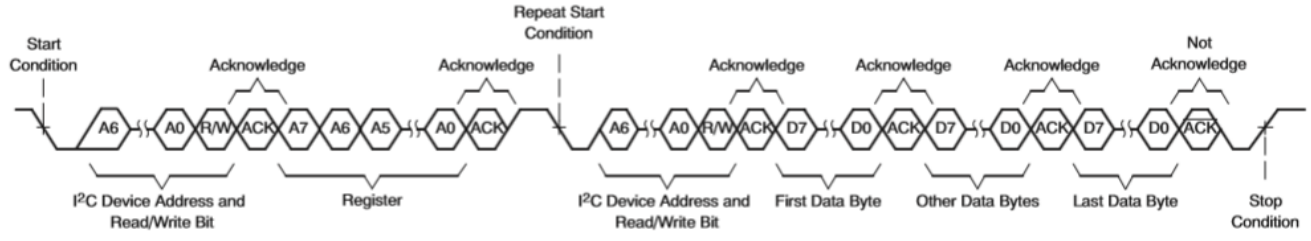


Figure 9 Multiple-Byte Read Transfer

4 Register Map

Table. 6 Register Map

Category	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default Value
Analog registers	0x00	Reserved	Step Pace	LIM	TFB_EN	TFB Attack Time t_{A_TFB}		TFB Release Time t_{R_TFB}		1Ah
	0x01	AGC Attack Time t_{A_AGC}				AGC Release Time t_{R_AGC}				97h
	0x02	Reserved		Analog Gain						26h
	0x03	Modulation	FREQ [1:0]		OCE_{Th}		OTE	OCE	DCE	27h
Analog registers with digital buffers	0x04	ADR	GAIN [1:0]		FREQ [2]	PBTL	CLKE	Reserved	MuteA	71h
	0x05~0x0F	Reserved								
Digital registers	0x10	DigClip[19:12]								FFh
	0x11	DigClip[11:4]								FFh
	0x12	DigClip[3:0]				SLEEP	SD	MUTE_L	MUTE_R	F4h
	0x13	Left channel volume control Vol_L								CFh
	0x14	Right channel volume control Vol_R								CFh
	0x15	Fade	HPF Byps	Dig Bst[1:0]		SS/DS	Serial Audio Input Format			94h
	0x16	PBTL_ch	Reserved							A0h

Notice that these registers falls into 3 different categories with different reading/writing requirements.

Category-1: analog registers from 0x00 to 0x03

The analog registers can be read and written only when HT5606 is powered on and not in shutdown mode. The settings in registers from 0x00 to 0x03 belong to the analog circuits of HT5606. In shutdown mode, the analog circuits are disabled and these analog registers cannot be written or read. Write these analog registers after HT5606 is enabled from shutdown mode and after 30ms setup time for the analog circuits.

Category-2: analog register with digital buffer 0x04

The register 0x04 can be written but not read when HT5606 is in shutdown mode. The settings in register 0x04 also belong to the analog circuits of HT5606, however, corresponding buffer is designed for each writable bit in digital circuits. These buffers can be written in shutdown mode and automatically transfer to the register 0x04 after HT5606 is enabled from shutdown mode.

Make sure that the bit3 PBTL is written properly before the analog circuits of HT5606 is enabled if the output terminal is paralleled in PBTL mode (that is to write the bit3 PBTL in register 0x04 into "1" after HT5606 is powered on and still in shutdown mode, if HT5606 is set in PBTL mode), so as to avoid over current protection once the HT5606 is enabled from shutdown mode.

注意，这些寄存器分为 3 个不同的类别，具有不同的读/写要求。

分类 1：模拟寄存器，0x00~0x03

模拟寄存器只能在 HT5606 上电且不处于关机模式时读取和写入。从 0x00 到 0x03 的寄存器设置属于 HT5606 的模拟电路。在关机模式下，模拟电路被禁用，这些模拟寄存器不能被写入或读取。在 HT5606 从关闭模式启用并且经过 30ms 的模拟电路启动时间后，写入这些模拟寄存器。

分类 2：具有数字缓存的模拟寄存器：0x04

当 HT5606 处于关闭模式时，寄存器 0x04 可以写入，但不能读取。寄存器 0x04 中的设置也属于 HT5606 的模拟电路，但是，其在数字电路中设计了相应的缓冲器。这些缓冲器可以在关机模式下写入，并在 HT5606 从关机模式启用后自动传输到寄存器 0x04。

如果输出端并联在 PBTL 模式下，则在 HT5606 的模拟电路启用之前，确保 bit3 PBTL 写入正确，（即 HT5606 通电后仍处于关机模式，如果 HT5606 设置为 PBTL 模式，则寄存器 0x04 中的 bit3 PBTL 写入 "1"），以避免 HT5606 启动后出现过流保护。

Category-3: digital registers from register 0x10 to register 0x16

The digital registers can be read and written while HT5606 is powered on, even if it is in shutdown mode. The settings in registers from 0x10 to 0x16 belong to the digital circuits of HT5606. Since HT5606 is powered on, even if it is in shutdown mode, the digital circuits are enabled and these digital registers can be written and read.

The register details are as follows. The blue fonts are the default settings when powering on.

分类 3：数字寄存器，0x10~0x16

数字寄存器可以在 HT5606 通电时读写，即使它处于关机模式。从 0x10 到 0x16 的寄存器设置属于 HT5606 的数字电路。由于 HT5606 已通电，即使处于关机模式，也会启用数字电路，可以写入和读取这些数字寄存器。

寄存器详情如下。蓝色字体是开机时的默认设置。

Register Address: 0x00 (default 1Ah)

Bit	R/W	Label	Default	Description	
7	/	Reserved	0	Unused	
6	R/W	Step Pace	0	0: 80 steps,0.25db/step 1: 40 steps,0.5db/step	
5	R/W	LIM	0	Power Limit Mode 0: PCLP function enabled; 1: AGC function enabled	
4	R/W	TFB_EN	1	0: TFB function disabled; 1: TFB function enabled	
3:2	R/W	t_{A_TFB}	10	Thermal Foldback (TFB) Attack Time Setting	
				00: 320ms/step	10: 1280ms/step
				01: 640ms/step	11: 2560ms/step
1:0	R/W	t_{R_TFB}	10	Thermal Foldback (TFB) Release Time Setting	
				00: 640ms/step	10: 2560ms/step
				01: 1280ms/step	11: 5120ms/step

Register Address: 0x01 (default 97h)

Bit	R/W	Label	Default	Description			
7:4	R/W	t_{A_AGC}	1001	AGC Attack Time Setting			
				0000	20μs/step	1000	5.12ms/step
				0001	40μs/step	1001	10ms/step
				0010	80μs/step	1010	20ms/step
				0011	160μs/step	1011	40ms/step
				0100	320μs/step	1100	80ms/step
				0101	640μs/step	1101	Reserved
				0110	1.28ms/step	1110	Reserved
				0111	2.56ms/step	1111	Reserved
3:0	R/W	t_{R_AGC}	0111	AGC Release Time Setting			
				0000	1.28ms/step	1000	1.28ms/step
				0001	2.56ms/step	1001	2.56ms/step
				0010	5.12ms/step	1010	5.12ms/step
				0011	10ms/step	1011	10ms/step
				0100	20ms/step	1100	20ms/step
				0101	40ms/step	1101	Reserved
				0110	80ms/step	1110	Reserved
				0111	160ms/step	1111	Reserved

Note: Do make sure that the release time is longer than attack time.

Register Address: 0x02 (Default 26h)

Bit	R/W	Label	Default	Description
7:6	/	Reserved	00	Unused, make it always 00
5:0	R/W	Analog Gain	26h	Set analog gain: 00,0000: 6dB 00,0001: 6.5dB ....Gain increased by ~0.5dB per step 10,0110:25dB ....Gain increased by ~0.5dB per step 11,1100: 36dB

Register Address: 0x03 (default 27h)

Bit	R/W	Label	Default	Description	
7	R/W	Modulation	0	0: BD mode; 1: 1SPW mode	
6:5	R/W	FREQ[1:0]	01	The amplifier PWM frequency is set by two registers: FREQ [1:0] and FREQ [2]	
4:3	R/W	OCE_{TH}	00	OCE Threshold Setting	
				00:10A	10: 7.5A
				01: 5A	11: 2.5A
2	R	OTE	1	Changes to 0 when OTE happened; back to 1 when OTP evacuated;	
1	R	OCE	1	Changes to 0 when OCE happened; back to 1 when OCP evacuated;	
0	R	DCE	1	Changes to 0 when DCE happened; back to 1 when DCP evacuated;	

Register Address: 0x04 (default 71h)

Bit	R/W	Label	Default	Description	
7	R	ADR	0	0: SLEEP/ADR = L; 1: SLEEP/ADR = H	
6:5	R	GAIN [1:0]	11	Analog Gain Setting, depends on 0x02	
4	R/W	FREQ [2]	1	The amplifier PWM frequency is set by two registers: FREQ [1:0] and FREQ [2]. Please notice that a PWM frequency between 300kHz and 600kHz will get a better performance for the Class D amplifier. Detailed recommendations for the SPK_CLK selection are listed in Table. 7. The following is the setting for FREQ [2:0]	
				000: FREQ = 6*fs	001: FREQ =8*fs
				010: FREQ =10*fs	011: FREQ =12*fs
				100: FREQ =14*fs	101: FREQ =16*fs
				110: FREQ =20*fs	111: FREQ =24*fs
3	R/W	PBTL	0	0: BTL mode; 1: PBTL mode.	
2	R	CLKE	0	Changes to 1 when CLKE happened; back to 0 when CLKE evacuated;	
1	/	Reserved	0	Unused	
0	R/W	MUTEA	1	Analog OUTPUT MUTE. When set 0, MUTE the SPEAKER OUTPUT.	

Table. 7 Recommendations for the FREQ Selection

fs(kHz)	Recommended FREQ	Recommended Amplifier Switching (PWM) frequency (kHz)
12	24*fs	288
16	24*fs	384
24	16*fs	384
32	12*fs	384
38	10*fs	380
44.1	8*fs	352.8
48	8*fs	384
88.2	8*fs	352.8
96	8*fs	384

Register Address: 0x10 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[19:12]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

Register Address: 0x11 (default FFh)

Bit	R/W	Label	Default	Description
7:0	R/W	DigClip[11:4]	FFh	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.

The digital clipper level determined by DigClip[19:0] is the maximum output threshold level from DAC transferring to the analog Amplifier. The default value of the digital clipper level is the full scale of DAC output, and decreasing the value of DigClip[19:0] will decrease the digital clipper level as well.

Register Address: 0x12 (default F4h)

Bit	R/W	Label	Default	Description
7:4	R/W	DigClip[3:0]	1111	The digital clipper level is decoded from 3 registers: DigClip[19:12], DigClip[11:4] and DigClip[3:0]. The default value is the highest value of the level.
3	R/W	SLEEP	0	0: the device is not in the SLEEP mode; 1: the device is in the SLEEP mode.
2	R/W	SD	1	0: the device is shut down; 1: the device is not shut down;
1	R/W	MUTE_L	0	MUTE the L channel digital output: 0: the left channel is not muted 1: the left channel is muted
0	R/W	MUTE_R	0	MUTE the R channel digital output: 0: the right channel is not muted 1: the right channel is muted

Register Address: 0x13 (Default CFh)

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_L	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB ……Gain decreased by 0.5dB every step 1100,1111: 0dB ……Gain decreased by 0.5dB every step 0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

Register Address: 0x14 (Default CFh)

Bit	R/W	Label	Default	Description
7:0	R/W	Vol_R	CFh	Left channel Volume control 1111,1111: +24dB; 1111,1110: 23.5dB ……Gain decreased by 0.5dB every step 1100,1111: 0dB ……Gain decreased by 0.5dB every step 0000,0111: -100dB Any setting less than 0000,0111 places the channel in MUTE

Register Address: 0x15 (default 94h)

Bit	R/W	Label	Default	Description
7	R/W	Fade	1	0: Volume fading is disabled; 1: Volume fading is enabled
6	R/W	HPF Byps	0	0: The internal high-pass filter in the digital path is not bypassed 1: The internal high-pass filter in the digital path is bypassed
5:4	R/W	Dig Bst	01	Digital Boost setting 00: +0dB is added to the signal in the digital path 01: +6dB is added to the signal in the digital path 10: +12dB is added to the signal in the digital path 11: +18dB is added to the signal in the digital path
3	R/W	SS/DS	0	Single Speed / Double speed mode select 0: Serial Audio Port will accept single speed sample rates (that is 32kHz, 44.1kHz, 48kHz) 1: Serial Audio Port will accept double speed sample rates (that is 88.2kHz, 96kHz)
2:0	R/W	Format	100	Serial Audio Input Format 000: Serial audio input format is 24 bits, right justified 001: Serial audio input format is 20 bits, right justified 010: Serial audio input format is 18 bits, right justified 011: Serial audio input format is 16 bits, right justified 100: Serial audio input format is IIS 101: Serial audio input format is 16-24 bits, left justified Settings above 101 are reserved and must not be used

Register Address: 0x16 (Default A0h)

Bit	R/W	Label	Default	Description
7	R/W	PBTL_ch	1	Channel selection for PBTL mode 0: the audio information from the left channel of the serial audio input stream is used 1: the audio information from the right channel of the serial audio input stream is used
6:0	/	Reserved	20h	Unused, make it always 20h.

5 Typical Applications

5.1 Hardware Control Mode

5.1.1 Startup Procedures

1. Configure all hardware pins as required by the application using PCB connections (that is PBTL, FREQ, GAIN, SLEEP, etc.)
2. \SD pin = Low;
3. Bring up power supplies (it does not matter if PVDD, AVDD or DVDD comes up first, provided the device is held in shutdown);
4. Once power supplies are stable, start MCLK, SCLK, LRCK;
5. Once power supplies and clocks are stable and the control port has been programmed, bring \SD pin High;
6. The device is now in normal operation. Fade in SDIN if needed

The sequence diagram is shown in Figure 10 and Table 9.

1. 设置所有IO口配置（如PBTL, RREQ, GAIN, SLEEP等）；
2. \SD脚拉低;
3. 接入电源（器件关断状态下，PVDD、AVDD、DVDD上电先后顺序无严格要求);
4. 当电源稳定后，开启MCLK, SCLK, LRCK;
5. \SD脚拉高;
6. 器件进入正常工作模式。若需要可将SDIN通过渐变引入。

具体时序如下图 Figure 10和下表Table 9.

5.1.2 Power down Procedures

1. The device is in normal operation;
2. Fade out SDIN if needed;
3. Pull \SD pin Low;
4. The clocks can be stopped, and power supplies brought down;
5. The device is now fully shutdown and powered off.

The sequence diagram is shown in Figure 11 and Table 10.

1. 芯片处于工作状态;
2. 若需要可将SDIN淡出；
3. 将\SD脚拉低;
4. MCLK, SCLK, LRCK关闭，然后电源关闭;
5. 芯片已关闭.

具体时序如下图 Figure 11和Table 10.

5.2 I²C Control Mode

5.2.1 Startup Procedures

1. Configure all digital I/O pins as required by the application using PCB connections (GAIN[1:0] = 11, ADR)
2. \SD pin = Low;
3. Bring up power supplies (it does not matter if PVDD, AVDD or DVDD comes up first, provided the device is held in shutdown);
4. Once power supplies are stable, start MCLK, SCLK, LRCK;
5. Configure the device via the control port in the manner required by the use case, making sure to mute the device; especially bit “PBTL” and “FREQ”. For instance, if BTL mode is needed, write the register 0x04 into 61h; if PBTL mode is needed, write the register 0x04 into 69h; if fs = 96kHz is needed, write the register 0x15 into 0x9C;
6. Once power supplies and clocks are stable and the control port has been programmed, bring \SD pin High;
7. The device is now in normal operation. Fade in SDIN if needed.

The sequence diagram is shown in Figure 10 and Table 9.

1. 设置所有IO口配置（GAIN[1:0]＝11, ADR）；
2. \SD脚拉低;
3. 接入电源（器件关断状态下，PVDD、AVDD、DVDD上电先后顺序无严格要求);
4. 当电源稳定后，开启MCLK, SCLK, LRCK;
5. 按照实际使用条件，通过控制端口配置器件，确保设备静音；特别是位“PBTL”和“FREQ”。例如，如果需要BTL模式，将寄存器0x04写入61h；如果需要PBTL模式，将寄存器0x04写入69h；如果需要fs=96kHz，将寄存器0x15写入0x9C；
6. \SD脚拉高;
7. 器件进入正常工作模式。若需要可将SDIN通过渐变引入。此后仍可通过IIC进行部分配置。（下图中的“B”）

具体时序如下图 Figure 10和下表 Table 9.

5.2.2 Power down Procedures

1. The device is in normal operation;
2. Fade out SDIN if needed;
3. Pull \SD pin Low;
4. The clocks can be stopped, and power supplies brought down;
5. The device is now fully shutdown and powered off.

The sequence diagram is shown in Figure 11 and Table 10.

1. 芯片处于工作状态;
2. 若需要可将SDIN淡出；
3. 将\SD脚拉低;
4. MCLK, SCLK, LRCK关闭，然后电源关闭;
5. 芯片已关闭.

具体时序如下图 Figure 11和Table 10.

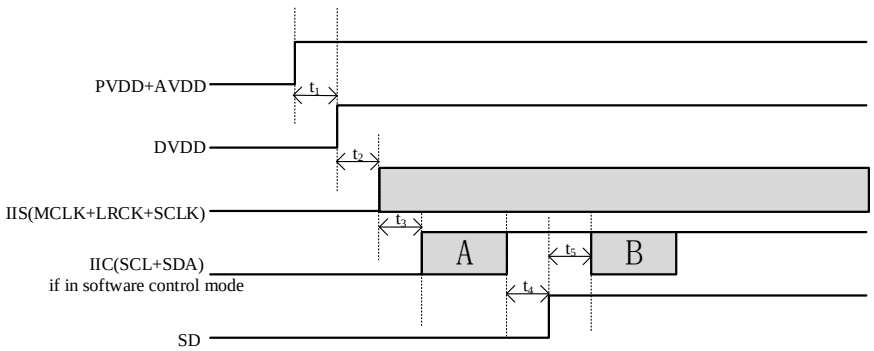


Figure 10 Power-on Sequence

Table. 8 Recommendations for Power-on Timing

Symbol	CONDITION	MIN	TYP	MAX	UNIT
t1		0			ms
t2		0			ms
t3		1			ms
t4		1			ms
t5		30			ms

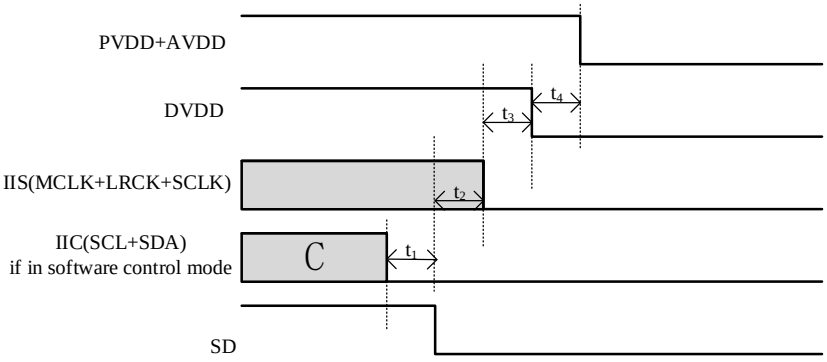


Figure 11 Power-off Sequence

Table. 9 Recommendations for Power-off Timing

Symbol	CONDITION	MIN	TYP	MAX	UNIT
t_1		1			ms
t_2	Fade-out disabled	1			ms
	Fade-out enable	45			ms
t_3		1			ms
t_4		0			ms

5.2.3 Fade-in and Fade-out

A (see in Figure 14): set work mode

Set a low-level digital gain: for example, write 0x13 and 0x14 into 0x9F;

Set BTL or PBTL, set Class D frequency, mute analog output: For BTL, write 0x04 into 0x61; For PBTL, write 0x04 into 0x69;

Set SS or DS: for 48k FS, write 0x15 into 0x94; For 96k FS, write 0x15 into 0x9C;

B (see in Figure 14): Fade-in

Increase digital gain to target gain by steps: For example, the target digital gain is 0dB(write 0x13 and 0x14 into 0xCF), write register 0x13 and 0x14 from 0x9F to 0xCF by steps, increase per 20ms.

C (see in Figure 15): Fade-out

Decrease digital gain by steps: For example, write register 0x13 and 0x14 from 0xCF to 0x9F by steps, decrease per 20ms.

Disable analog output: write 0x04 into 0x60 for BTL; write 0x04 into 0x68 for PBTL.

A（见图14）：设置工作模式

设置一个低数字增益：例如，将0x13和0x14写入0x9F；

设置BTL或PBTL，设置D类频率，模拟输出静音：BTL将0x04写入0x61；PBTL将0x04写入0x69；

设置SS或DS：对于48k FS，将0x15写入0x94；对于96k FS，将0x15写入0x9C；

B（见图14）：淡入

将数字增益递增到目标增益：例如，目标数字增益为0dB（将0x13和0x14写入0xCF），将寄存器0x13和0x14从0x9F递增到0xCF，每20ms递增一次。

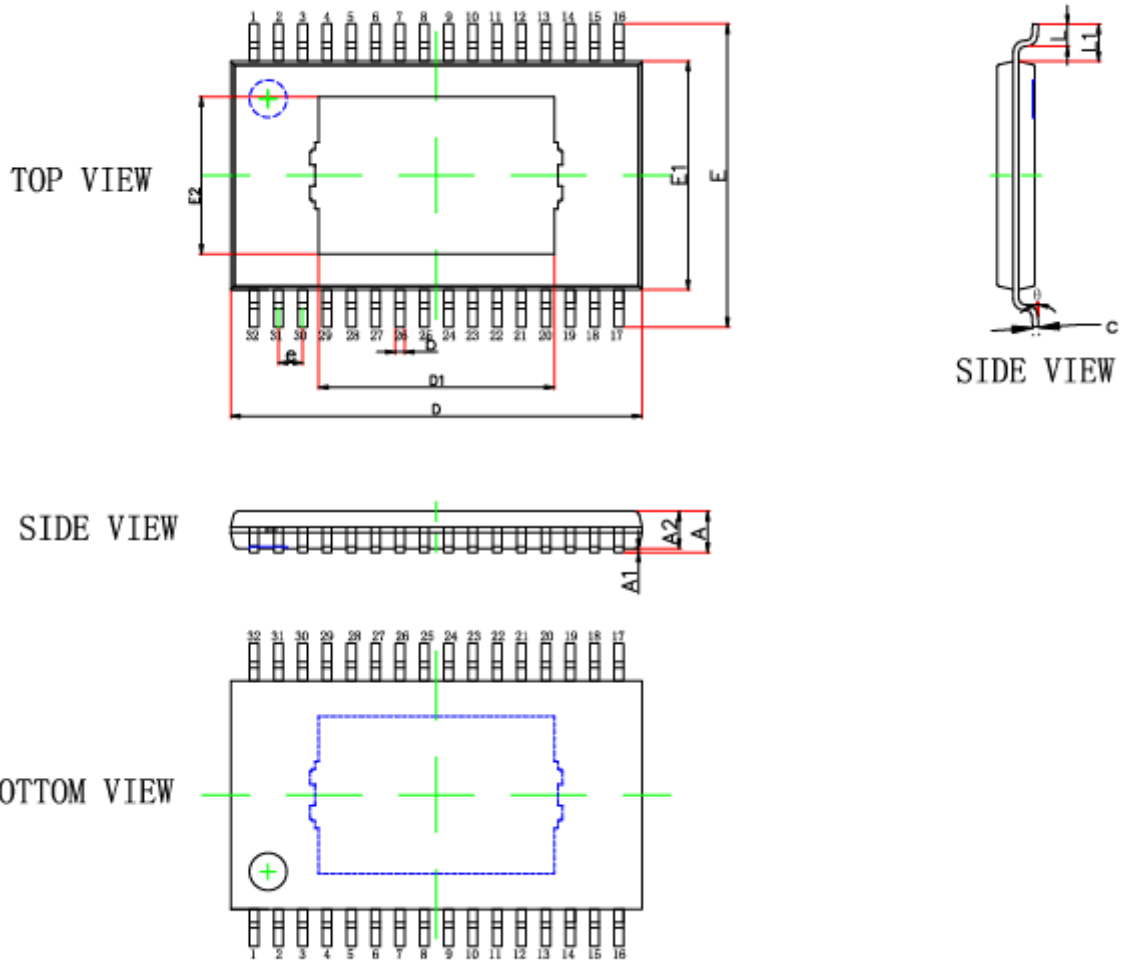
C（见图15）：淡出

数字增益递减：例如，将寄存器0x13和0x14从0xCF递增写入0x9F，每20ms递减一次。

禁用模拟输出：BTL将0x04写入0x60；PBTL将0x04写入0x68.

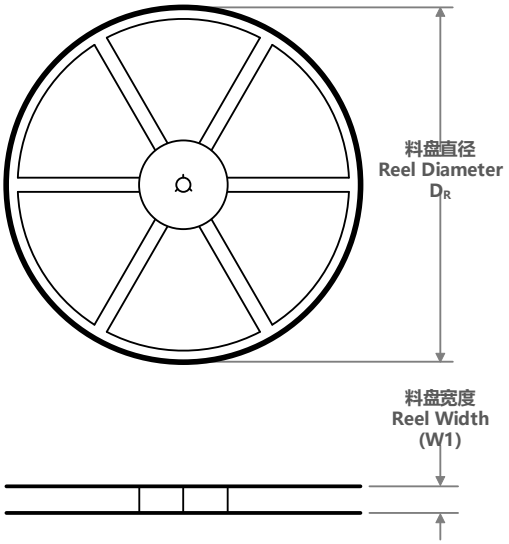
■ PACKAGE OUTLINE

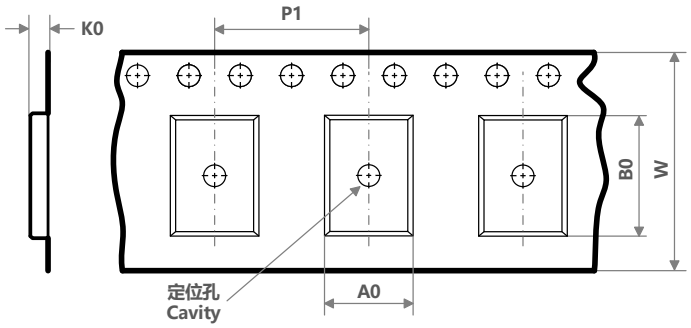
ETSSOP32 (EPAD up)



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	NOM	Max.	Min.	NOM	Max.
A	—	—	1.200	—		0.047
A1	0.000	0.075	0.150	0.000	0.003	0.006
A2	0.900	1.000	1.100	0.035	0.039	0.043
b	0.200	—	0.280	0.008	—	0.011
c	0.150	—	0.190	0.006	—	0.007
D	10.900	11.000	11.100	0.429	0.433	0.437
D1	6.200	6.300	6.400	0.244	0.248	0.252
E	7.900	8.100	8.300	0.311	0.319	0.327
E1	6.000	6.100	6.200	0.236	0.240	0.244
E2	4.100	4.200	4.300	0.161	0.165	0.169
e	0.650(BSC)			0.026(BSC)		
L	0.500	0.625	0.750	0.020	0.025	0.030
θ	0°		8°	0°		8°

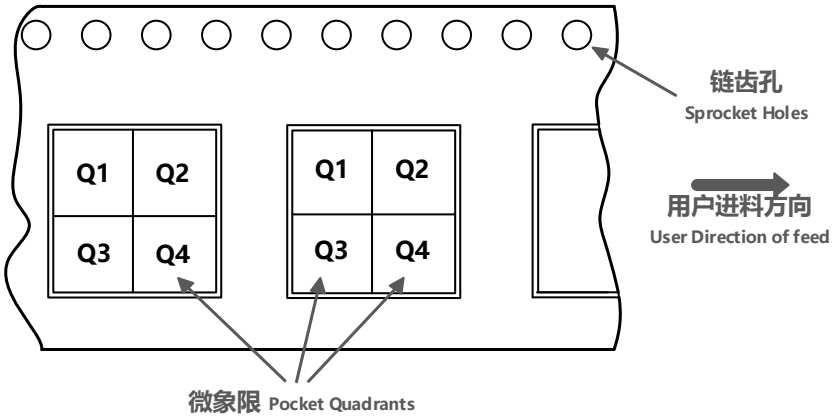
■ TAPE AND REEL INFORMATION





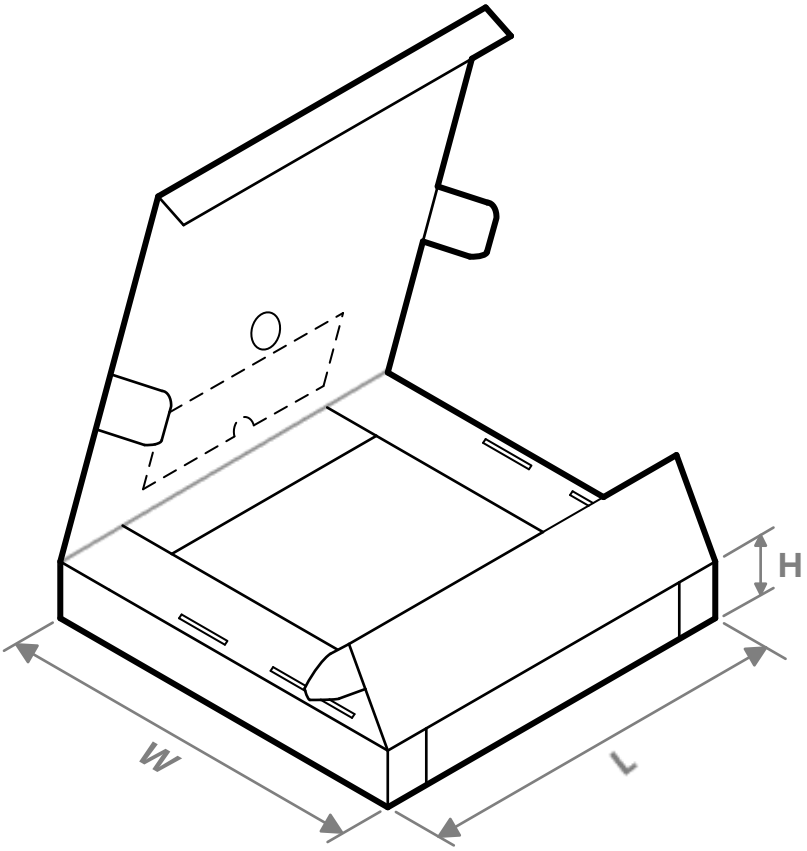
A0	Dimension designed to accommodate the component width; 料槽宽度
B0	Dimension designed to accommodate the component length; 料槽长度
K0	Dimension designed to accommodate the component thickness; 料槽厚度
W	Overall width of the carrier tape; 载带整体宽度
P1	Pitch between successive cavity centers; 相邻槽中心间距

编带 PIN1 方位象限分配
Quadrant Assignments for Pin1 Orientation in Tape



器件料号 Part No.	封装类型 Package Type	封装标识 Package Abbr.	引脚数 Pins	SPQ	料盘直径 D_R(mm)	料盘宽度 W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 象限 Quadrant
HT5606MTER	ETSSOP	MTE	32	2000	330	24.4	8.6	11.45	1.9	16	24	Q1

■ TAPE AND REEL BOX INFORMATION



器件料号 Part No.	封装类型 Package Type	封装标识 Package Abbr.	引脚数 Pins	SPQ	长度 Length (mm)	宽度 Width (mm)	高度 Height (mm)
HT5606MTER	ETSSOP	MTE	32	2000	336	336	48

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