AXPM65611

200mA Triple DC-DC Converter with LDO AVDD for Powering AMOLED Display

Datasheet — Sep 2023

Description

AXPM65611 is a triple DC-DC converter designed to drive AMOLED display panel requiring 3 supply rails. It integrates an 200mA step-up converter VPOS, an 200mA inverting converter VNEG and an 20mA auxiliary LDO AVDD. The device is particularly suitable for battery operated products, in which the major concern is the overall system efficiency. The digital control allows programming the VNEG in digital steps. Excellent line and load regulation, soft start with controlled inrush current limit, thermal shutdown and short circuit protection are also integrated.

Features

- Operating input voltage range from 2.9V to 4.5V
- Step-up converter (VPOS)
  - 4.6V output voltage
  - 200mA output current
  - 0.5% accuracy (25°C to 85°C)
- Inverting converter (VNEG)
  - -1.4V to -4.4V programmable output voltage (-2.2V default)
  - 200mA output current
- LDO (AVDD)
  - 3.3V default or lower of Vin
  - 20mA output current
- Efficiencies >90%
- Excellent line and load regulation
- Short circuit protection
- Thermal shutdown

Applications

- AMOLED power supply in portable devices like mobile phones, multi-media players, camcorders, digital still cameras, and wearables.

Table 1 Device Summary

Order code	Package	Packing	MOQ
AXPM65611	DFN12 2.4 × 1.5 x 0.5mm	Reel	3000

DFN12 2.4 × 1.5 x 0.5mm

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Figure 1 Block Diagram

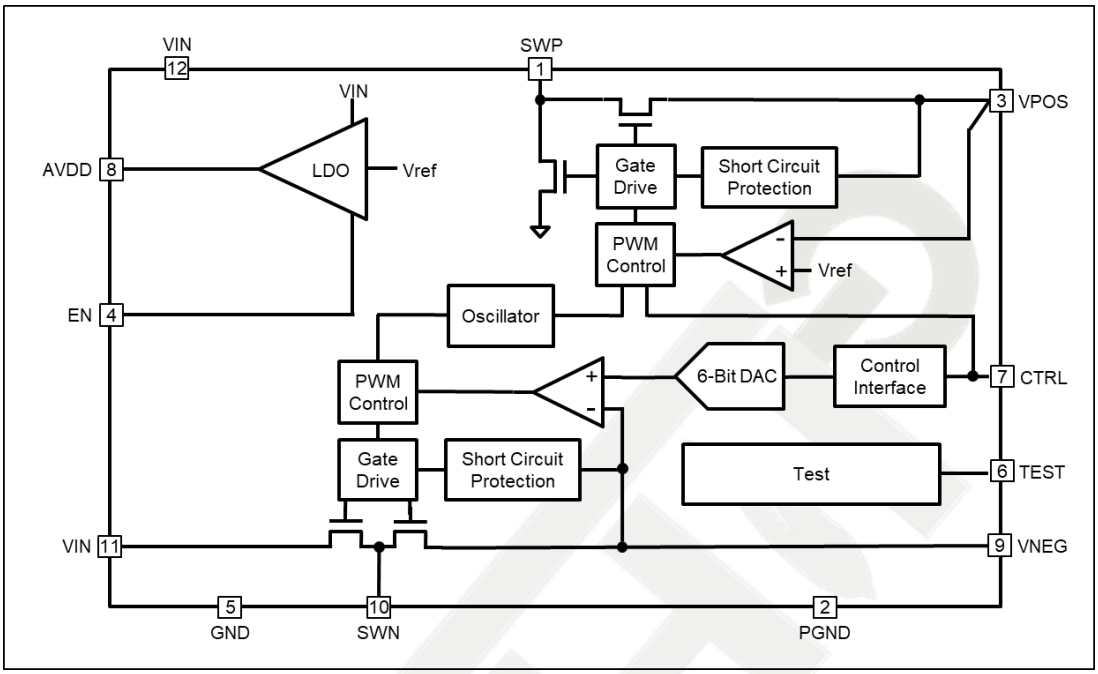
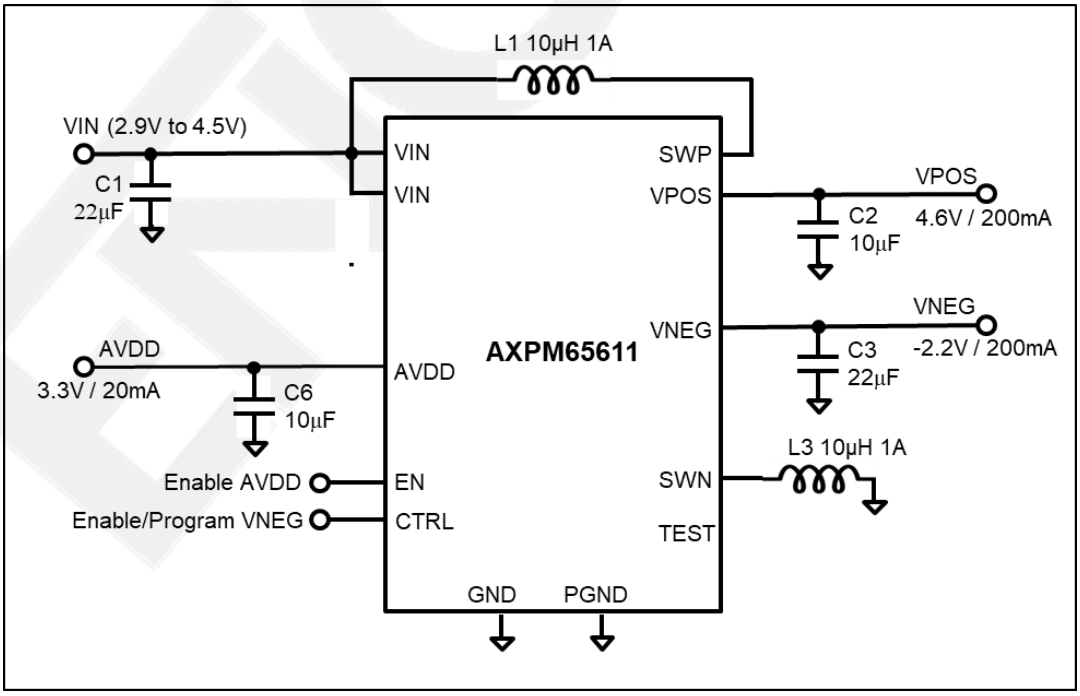


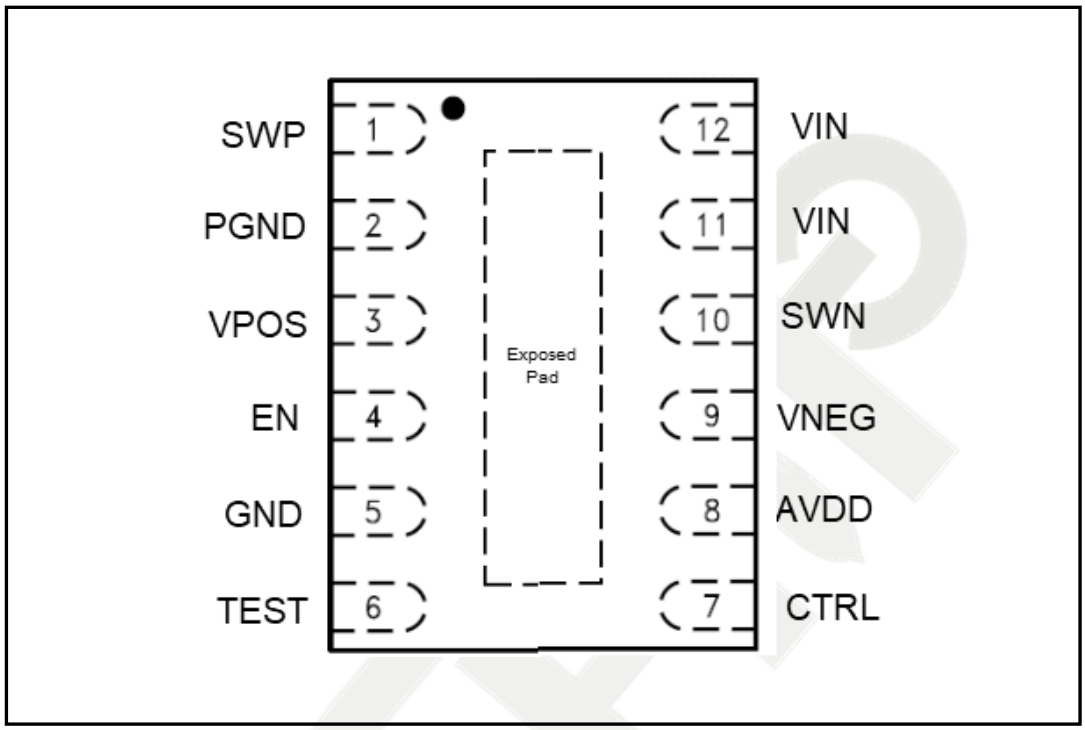
Figure 2 Application Circuit



2 Pin Description

2.1 Pin Names

Figure 3 Pin Connection



2.2 Pin Functions

Table 2 Pin Functions

Pin number	Pin name	Description
1	SWP	Step-up converter VPOS switch pin
2	PGND	Power Ground
3	VPOS	Step-up converter VPOS output
4	EN	AVDD Enable pin
5	GND	Analog Ground
6	TEST	Reserved for device testing. Not to be connected
7	CTRL	Step-up converter VPOS and VNEG enable/program pin
8	AVDD	3.3V AVDD
9	VNEG	Inverting converter VNEG output
10	SWN	Inverting converter VNEG switch pin
11	VIN	Power Supply
12	VIN	Power Supply
EPAD		Connect this pad to GND and PGND.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
SWP, VPOS, VIN	DC supply voltage, output voltage	-0.3 to +5.5	V
AVDD	Output voltage	-0.3 to +8.5	V
VNEG	Output voltage	-6.0 to +0.3	V
SWN	Switching node voltage	-6.5 to +4.8	V
CTRL, EN, TEST	Input logic voltage, analog input.	-0.3 to +5.5	V
Tj	Junction temperature	150	°C
Tstg	Storage temperature	-55 to +150	°C

3.2 Thermal Data

Table 4 Thermal Data

Symbol	Parameter	Value	Unit
Rth j-amb	Thermal resistance junction-to-ambient	48.8	°C/W
Rth j-case	Thermal resistance junction-to-case	2.6	°C/W

3.3 ESD and Latch Up

Table 5 ESD and Latch Up

Symbol	Parameter	Value	Unit
All pins	ESD HBM	±2,000	V
All pins	ESD CDM	±500	V
All pins	Latch Up JESD78, Class A	≥ 100	mA

3.4 Electrical Characteristics

VIN = 3.7V, CTRL = 3.7V, EN = 3.7V, VPOS = +4.6V, VNEG = -2.2V,
AVDD = +3.3V, typical values are at T_A = 25°C (unless otherwise noted).

Table 6 Electrical Characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
General						
VIN	Supply input voltage		2.9	3.7	4.5	V
Temp	Operating temperature		-40	25	85	°C
I_{SD}	Shutdown current	CTRL=GND EN=GND			1	μA
V_{UVLO}	Under-voltage lockout threshold	VIN Falling		2.1		V
		VIN Rising		2.3		V
Logic Signals (CTRL, EN)						
V_H	High Threshold	VIN=2.9 to 4.5V	1.2			V
V_L	Low Threshold				0.4	V
R_{DOWN}	Pull-down resistance			300		kΩ
Step-up Converter (VPOS)						
VPOS	Positive output voltage			4.6		V
	Positive output voltage variation	25°C≤T_A≤ 85°C No load	-0.5		+0.5	%
		–30°C≤T_A≤ 85°C No load	-0.8		+0.8	%
	Line regulation	I_{VPOS}=200mA		2		mV
	Load regulation	1mA≤ I_{VPOS} ≤200mA		2		mV
$R_{DS(on)1A}$	Switch on-resistance	I_{SWP1}=200mA		200		mΩ
$R_{DS(on)1B}$	Rectifier on-resistance			600		mΩ
f_{SW1}	Switching frequency	I_{VPOS} =200mA		1.5		MHz
I_{SW1}	Switch current limit	Inductor valley current		1.0		A
I_{O1MAX}	Maximum output current	VIN=2.9V to 4.5V	200			mA
V_{SCP1}	Short circuit threshold in operation	VPOS falling		85% of VPOS		
t_{SCP1}	Short circuit detection time in operation			3		ms
R_{DCHG1}	Discharge resistance	CTRL=GND I_{SWP1}=1mA		30		Ω
Inverting Converter (VNEG)						
VNEG	Output voltage default			-2.2		V
	Output voltage range		-1.4		-4.4	V
	Output voltage accuracy	25°C≤T_A≤ 85°C No load	-50		+50	mV
		–30°C≤T_A≤ 85°C No load	-60		+60	mV
	Line regulation	I_{VNEG}=200mA		2		mV
	Load regulation			2		mV
$R_{DS(on)2A}$	SWN mosfet on-resistance	I_{SWN}=200mA		200		mΩ
$R_{DS(on)2B}$	SWN mosfet rectifier on-resistance			300		mΩ

f_{SW2}	SWN Switching frequency	I_{VNEG} =10mA		1.5		MHz
I_{SW2}	SWN switch current limit	VIN=2.9V		1.2		A
I_{O2MAX}	Maximum output current	VIN=2.9V	-200			mA
V_{SCP2}	Short circuit threshold in operation	Voltage increase from nominal VNEG		85% of VNEG		V
	Short circuit threshold in start up			250		mV
t_{SCP2}	Short circuit detection time in start up			10		ms
	Short circuit detection time in operation			3		ms
R_{DCHG2}	Discharge resistance	CTRL=GND I_{SWN}=1mA		150		Ω
LDO (AVDD)						
AVDD	Output voltage	EN=1		3.3		V
	Output voltage accuracy	25°C≤T_A≤ 85°C No load	-1.0		+1.0	%
		–30°C≤T_A≤ 85°C No load	-1.3		+1.3	%
	Line regulation	I_{AVDD}=20mA		10		mV
	Load regulation			10		mV
R_{DCHG3}	Discharge resistance	EN=GND		250		Ω
Others						
t_{INIT}	Initialization time			300		µs
t_{STORE}	Data storage/accept time period		30	55	80	µs
T_{SDN}	Shutdown time period		30	55	80	µs
T_{SD}	Thermal shutdown temperature			145		°C
T_R	Thermal shutdown recovery temperature			130		°C
Timing Requirements CTRL Interface						
t_{LOW}	Low-level pulse duration		2	10	25	µs
t_{HIGH}	High-level pulse duration		2	10	25	µs

4 Functional Description

4.1 Overview

AXPM65611 is a high efficiency triple DC-DC converter consisting of 1 step-up converter,1 inverting converter and a AVDD LDO. The VPOS output is fixed at +4.6V and VNEG is programmable via a digital interface in the range of -1.4V to -4.4V; with default at -2.2V. AVDD is default set to 3.3V. The device has internal over-temperature protection, under voltage lockout and soft start which guarantees proper operation during start-up.

4.2 Step-up Converter (VPOS)

Step-up converter 1 uses a fixed-frequency current-mode topology. Its output voltage (VPOS) is programmed at the factory to 4.6V and cannot be changed by the user.

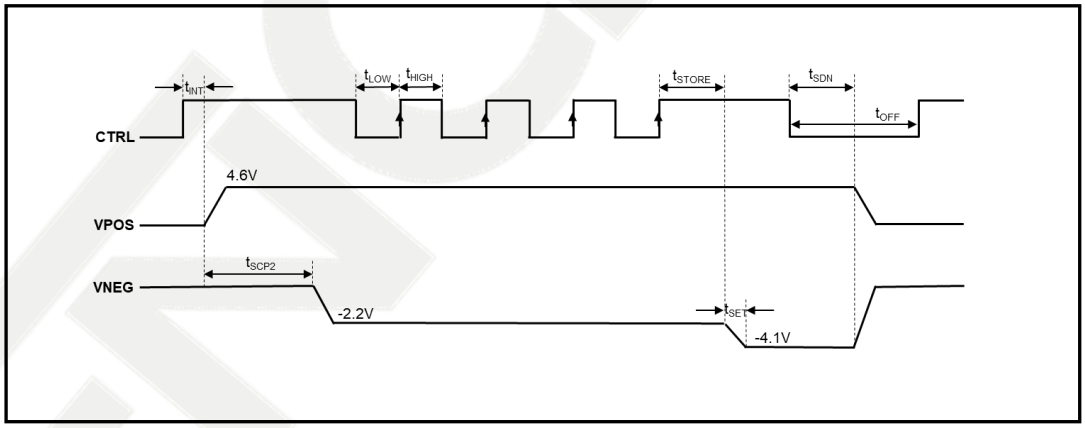
4.3 Inverting Converter (VNEG)

The inverting converter uses a constant-off-time current-mode topology. The converter's default output voltage (VNEG) is -2.2V. It can be programmed from -1.4 V to -4.4V.

4.3.1 Programming VNEG

The digital interface allows programming of VNEG in discrete steps. If the output voltage setting function is not required, then the CTRL pin can also be used as a standard enable pin. The digital output voltage programming of VNEG is implemented using a simple digital interface(SWIRE) with the timing shown in figure 4.

Figure 4 SWIRE Digital Interface Using CTRL



When CTRL is pulled high, the device starts up with its default voltage of -2.2 V. The device includes a 6-bit DAC that generates the output voltages shown in table 7. The interface counts the rising edges applied to the CTRL pin once the device is enabled. According to table 7, VNEG is programmed to -4.1V since 4 rising edges are detected.

Table 7 VNEG Programming by SWIRE

Pulse	VNEG (V)		Pulse	VNEG (V)
0	-2.2		16	-2.9
1	-4.4		17	-2.8
2	-4.3		18	-2.7
3	-4.2		19	-2.6
4	-4.1		20	-2.5
5	-4.0		21	-2.4
6	-3.9		22	-2.3
7	-3.8		23	-2.2
8	-3.7		24	-2.1
9	-3.6		25	-2.0
10	-3.5		26	-1.9
11	-3.4		27	-1.8
12	-3.3		28	-1.7
13	-3.2		29	-1.6
14	-3.1		30	-1.5
15	-3.0		31	-1.4

4.3.2 VNEG Transition Time

The transition time (t_{SET}) is the time required to move VNEG from one voltage level to the next. The transition time is designed for typical 300μs.

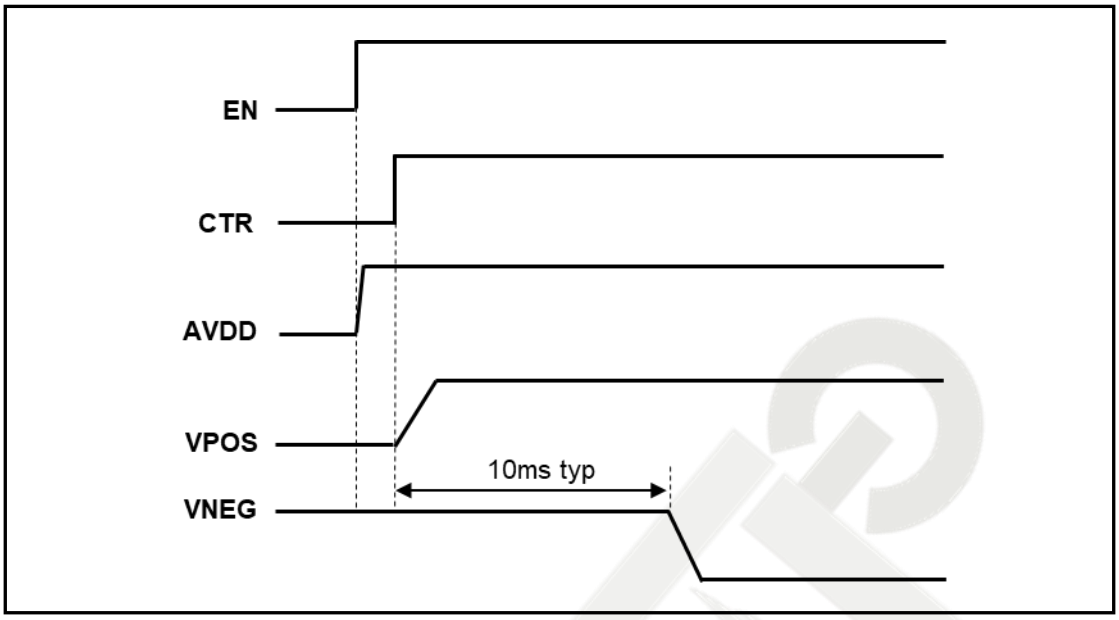
4.4 LDO (AVDD)

AVDD is derived from a LDO and can be enabled through the EN pin by connecting to high. In applications whereby the VIN pin falls below 3.3V, the AVDD output will follow the VIN input voltage.

4.5 Soft Start and Start-up Sequence

AXPM65611 features a soft-start function to limit inrush current. LDO (AVDD) is enabled when EN goes high. When CTRL goes high, step-up converter 1 starts with a reduced switch current limit and 10ms later the inverting converter starts with its default value of -2.2V. The typical start-up sequence is shown in Figure 5. The 2 step-up converters operate independently and step-up converter (VPOS) does not require LDO (AVDD) to be in regulation for it to start.

Figure 5 Start-up Sequence



4.6 VPOS and VNEG Enable (CTRL)

The CTRL pin serves two functions: one is to enable and disable the device VPOS and VNEG, and the other is to program the output voltage (VNEG) of the inverting buck-boost converter (see Programming VNEG). If the VNEG programming function is not required, the CTRL pin can be used as a standard enable pin for the device, which will start up with its default value of -2.2V on VNEG.

The device is enabled when CTRL is pulled high and disabled when CTRL is pulled low. Note that to ensure proper start up CTRL must be pulled low for a minimum of 200μs before being pulled high again.

4.7 Under-voltage Lockout

The device features an under-voltage lockout function that disables it when the input supply voltage is too low for proper operation.

4.8 Short Circuit Protection

4.8.1 Short Circuit During Operation

The device is protected against short circuit of VPOS and VNEG to ground and short circuit of these two outputs to each other. During normal operation, an error condition is detected if VPOS falls below 4.1V for longer than 3ms or VNEG is pulled above the programmed nominal output by 500mV for longer than 3ms. In either case the device goes into shutdown and the outputs are disconnected from the input. This state is latched, and to resume normal operation, VIN must cycle below the under-voltage lockout threshold, or CTRL must toggle LOW and then HIGH.

4.8.2 Short Circuit During Start-up

During start-up, an error condition is detected in the following cases:

- VPOS is not in regulation 10ms after CTRL goes HIGH.
- VNEG is higher than threshold level 10ms after CTRL goes HIGH.
- VNEG is not in regulation 20ms after CTRL goes HIGH.

If any of the above conditions is met the device goes into shutdown and the outputs are disconnected from the input. This state is latched, and to resume normal operation, VIN has to cycle below the undervoltage threshold, or CTRL has to toggle LOW and HIGH.

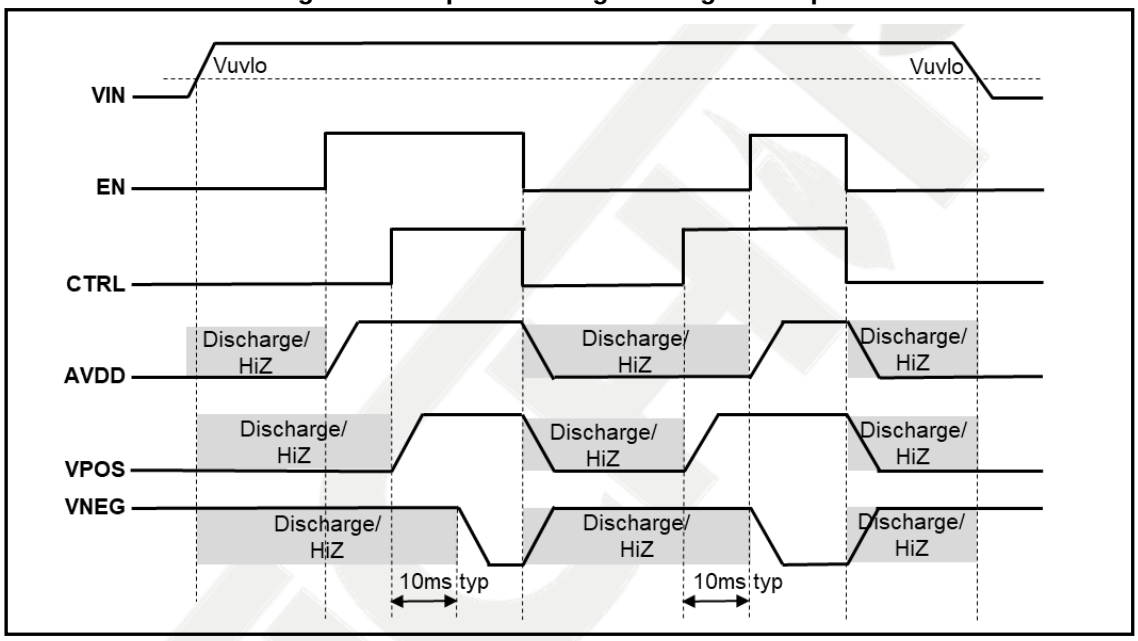
4.9 Output Discharge During Shut Down

The device outputs can be programmed for Discharge or HiZ during shutdown. Figure 6 shows the shutdown output control. Device is default programmed for Discharge during shutdown.

Table 8 Shutdown Output Programming by SWIRE

Pulse	Outputs
50	HiZ
51	Discharge

Figure 6 Output Discharge During Start-up



4.10 Device Functional Modes

4.10.1 Operation with VIN < 2.9V

The recommended minimum input supply voltage for full performance is 2.9V. The device continues to operate with input supply voltages below 2.9V but full performance is not guaranteed. It does not operate with input supply voltages below the UVLO threshold.

4.10.2 Operation with VI ≈ VPOS (Diode Mode)

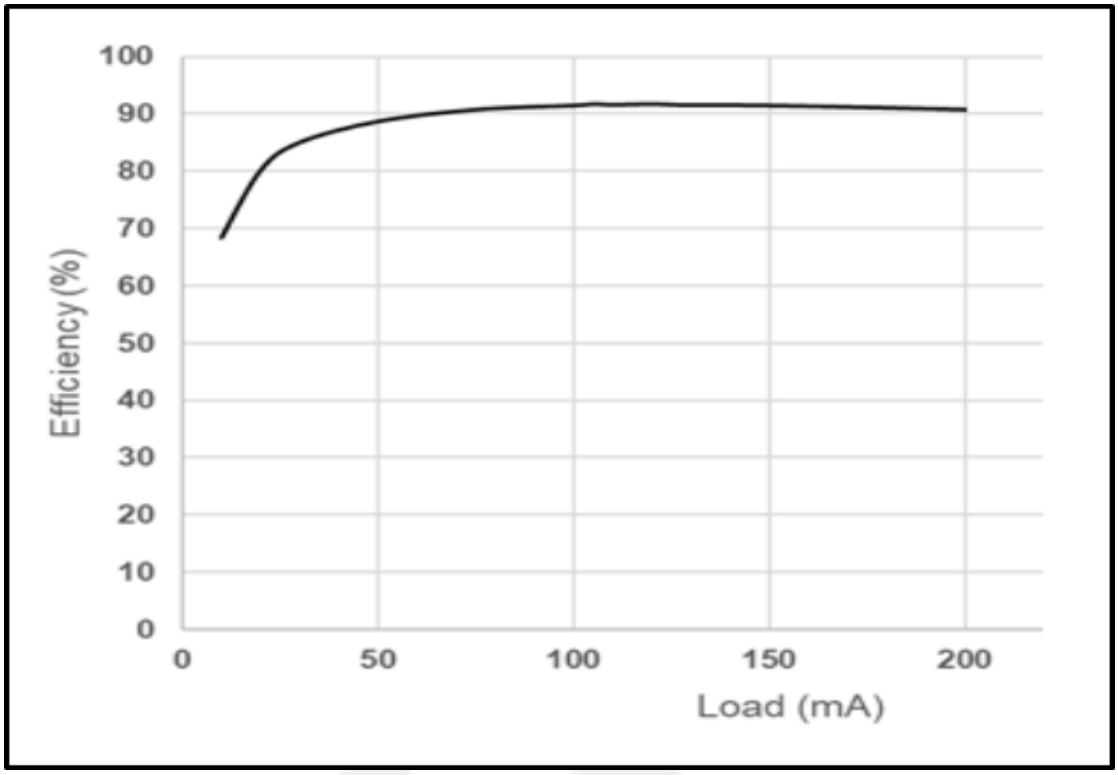
AXPM65611 features a "diode" mode that enables it to regulate its VPOS output even when the input supply voltage is close to VPOS (that is, too high for normal step-up operation). When operating in diode mode the VPOS boost converter's high-side switch is disabled and its body diode used as the rectifier. Note that a minimum load of ≈2mA is required to have proper output regulation in diode mode.

4.10.3 Operation with CTRL

When a low-level signal is applied to the CTRL pin the device is disabled and switching is inhibited. When the input supply voltage is above the UVLO threshold and a high-level signal is applied to the CTRL pin the device is enabled and its start-up sequence begins.

4.11 Typical Performances

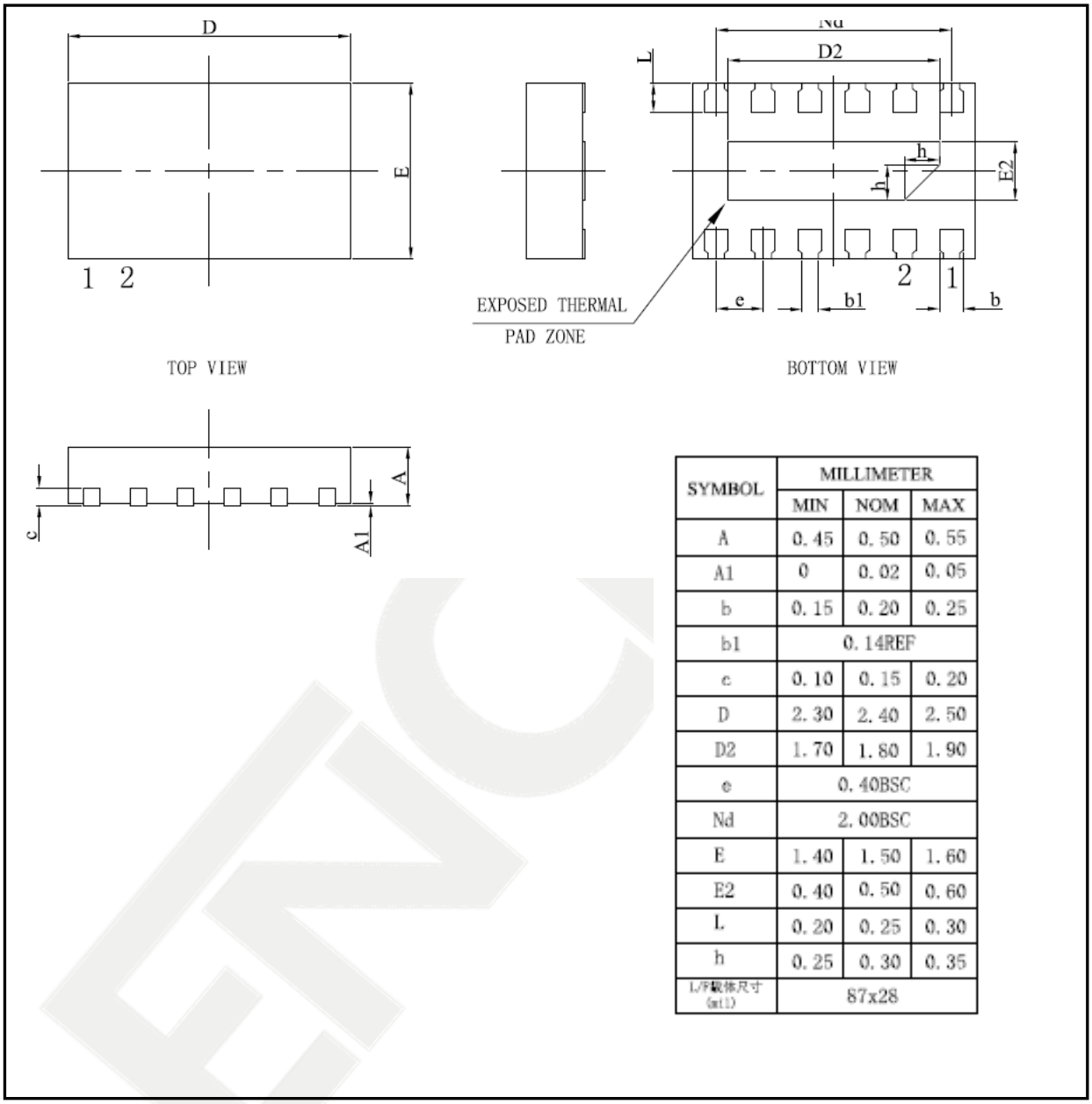
Figure 7 Efficiency vs Output Current (VPOS & VNEG)
(VIN = 3.7V, CTRL = 1, EN=1)



5 Package Information

5.1 Package Outline Dimensions

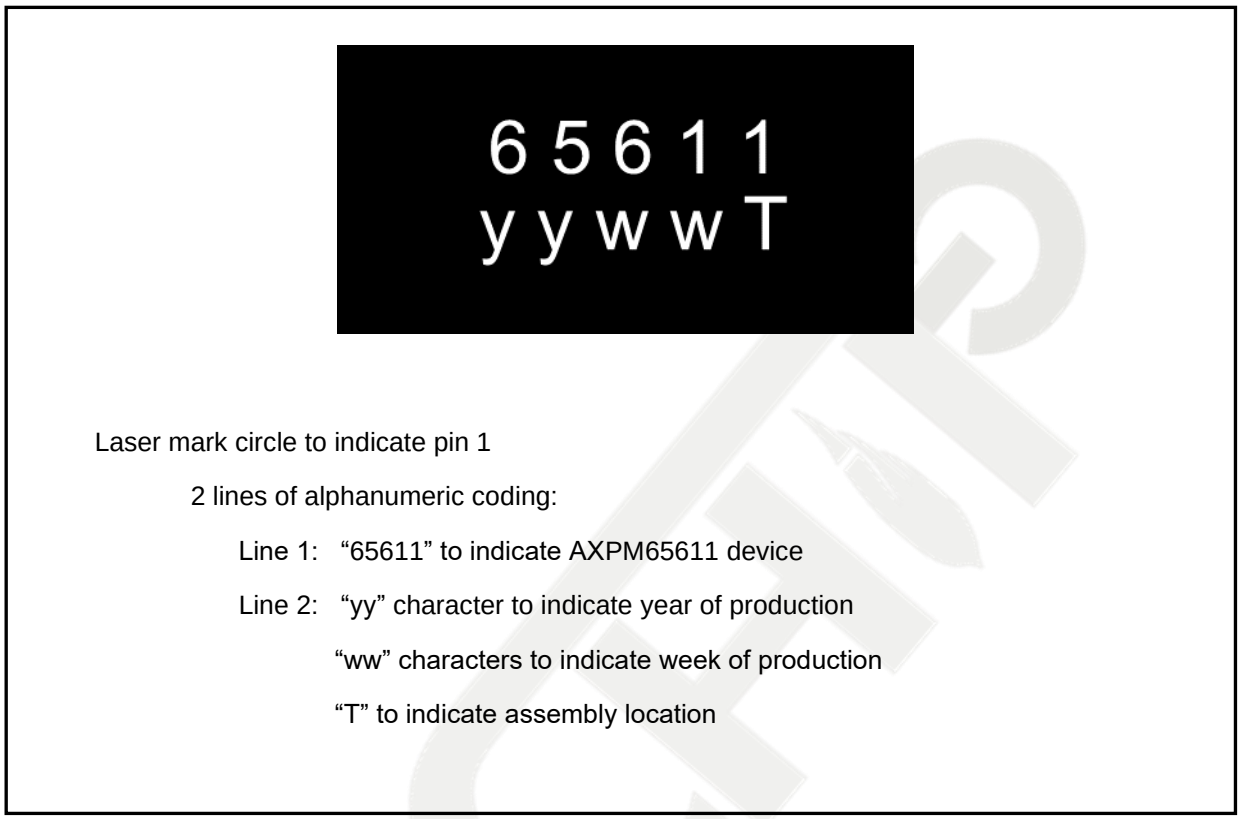
Figure 8 DFN12L 2.4 x 1.5 x 0.5mm Mechanical Data and Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.10	0.15	0.20
D	2.30	2.40	2.50
D2	1.70	1.80	1.90
e	0.40BSC		
Nd	2.00BSC		
E	1.40	1.50	1.60
E2	0.40	0.50	0.60
L	0.20	0.25	0.30
h	0.25	0.30	0.35
L/F载体尺寸 (mil)	87x28		

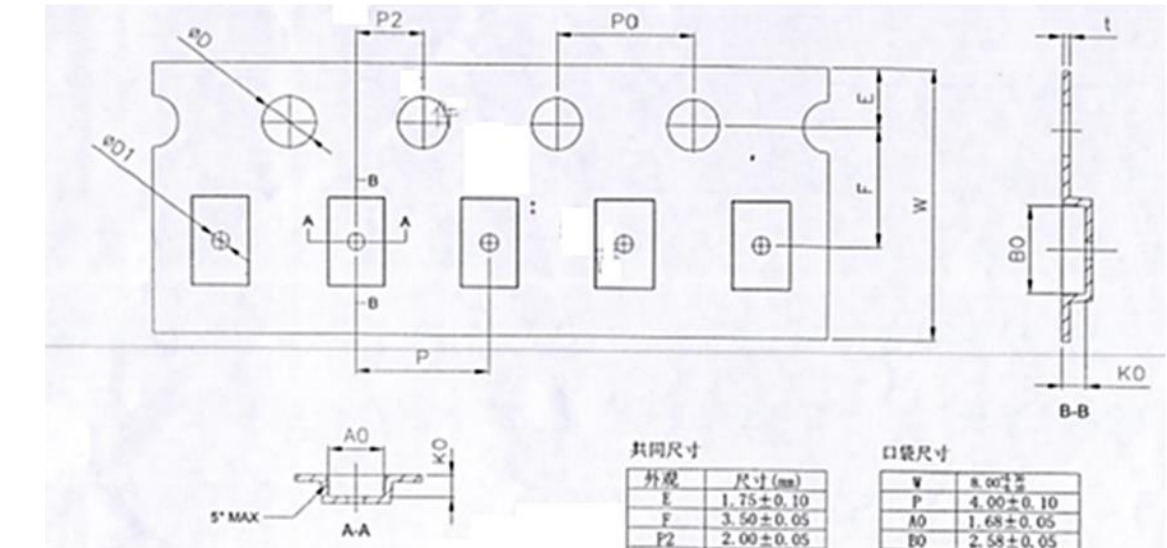
5.2 Package Marking Information

Figure 9 DFN12L 2.4 x 1.5 x 0.5 mm Marking Information



6 Packing Information

Figure 10 Reel Packing Information



共同尺寸

外观	尺寸(mm)
E	1.75±0.10
F	3.50±0.05
P2	2.00±0.05
D	1.50 +0.10
D1	0.50±0.05
P0	4.00±0.10
10P0	40.0±0.20

口袋尺寸

W	8.00 +0.30 -0.10
P	4.00±0.10
A0	1.68±0.05
B0	2.58±0.05
K0	0.65±0.05
t	0.20±0.02

技术要求:

1. 任意10个传输孔间距的累积误差±0.2mm;
2. 载带沿长度方向的侧弯≤1mm/100mm;
3. K0是从口袋的内部底面到载带的顶部表面测量的尺寸;
4. 表面电阻率: 10^5~10^9Ω/□;
5. 粗糙度: Ra＜0.8um;
6. 颜色: 黑色(参考色号:C0 M0 Y35 K100);

7 Revision History

Table 9 Document Revision History

Date	Version	Description
May 2022	1.00	First Version
Jun 2022	1.01	Application Diagram showing inductor rating as 10µH 1A
Aug 2022	1.10	Added Efficiency diagrams vs Inductor types
Mar 2023	1.11	Revised Line and Load regulation specification Corrected Typo in Application Diagram
Sep 2023	1.12	Revised Inductors